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"Execution of OFDM Transceiver using VHDL"

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Abstract:

Orthogonal frequency division multiplexing(OFDM)is a multicarrier modulation technique which isdeployed in modern communication systems because of its immunity to channel's harsh affects. The present standards use inbuilt IP's for the implementation of OFDM Transmitter and Receiver. This work provides the validation and implementation of OFDM Transceiver on FPGA which is completely digital, and the whole work is done using VHDL language. Field Programmable Gate Arrays provide the better platform for the variation of data rates and moreover they are of low cost, easily programmable. Software tools Radix-2 ifftbutterflyalgorithm is used to implement the IFFT block. The system isdesigned using VHDL and simulated using MODELSIM.

Keywords: **IFFT,FFT, OFDM, VHDL, QAM**

I.INTRODUCTION

In some applications, it is desirable to transmit the same information-bearing signal over several channels. This mode of transmission is used primarily in situations where there is high probability that one or more of the channels will be unreliable from time to time. One form of this multichannel signaling is sometimes employed in wireless communications systems as means of overcoming the effects of interference of the transmitted signal. By transmitting the same information over multiple-channels, provides signal diversity, which the receiver can exploit to recover the information. Another form of the multichannel communications in multiple carrier transmission, where the frequency band of the channel is subdivided into a number of sub-channels and information is transmitted on each of the subchannels. In non-ideal linear filter channels it is observed that such channels introduce ISI, which degrades performance compared with the idea channel. The degree of performance degradation depends on the frequencyresponse characteristics. Furthermore, the complexity of the receiver increases as the span of ISI increases. In this system, we consider the transmission of information on multiple carriers contained within the allocated channel bandwidth. The primary motivation for transmitting data on multiple carriers is to reduce ISI and thus, eliminate the performance degradation that is incurred in several methods to implement the system. One of such methods of implementing this system is by using FPGA (Field Programmable Gate Array).

OFDM, carried out in digital domain on FPGA, which is a programmable hardware and the full control over the actual design implementation resides with the user and there is no need for any physical IC fabrication facility. An FPGA with the programmability of a general purpose processor combines the speed, power and density attributes. This will be advantageous to the OFDM system implementation. To meet the future needs new functions should be added to the existing model and for this implementation FPGA is the better platform and can be easily fabricated to a chip. Thereby FPGA will be a good platform than any other for the OFDM implementation since it gives flexibility t the program design besides the low cost hardware component comparing to others.

II.IMPLEMENTATION OF OFDM TRANSCEIVER

A. OFDM TRANSMITTER BLOCKS

1) Input Sampler: The input sampler is the first block of the OFDM transmitter section. Serial data is fed as input to the block, and the output is a 2-bit IQ. The output is group of symbols, each containing two bits. So this input sampler is the block which groups two bits.

2) SYMBOL MAPPER: The output of the input sampler is fed as input to the symbol mapper. The symbol mapper consists of an QPSK modulator. The input 2-bit stream fed to the modulator divides it into two 2-bit symbols called I and Q (imaginary and quadrature). These symbols are generated based on the constellation diagram. In QPSK there are four phases, each 2-bit symbol is assigned to a phase, which are of 90 degrees difference between them. The coding is done based on the constellation diagram of QPSK

3) SERIAL INPUT PARALLEL OUTPUT (SIPO): This block's input is the output from the symbol mapper. SIPO, as the name indicates serial input parallel output, this block converts the serial data fed as input to parallel data. In this system, SIPO is a two 8 register (0-7) array. The serial input is fed at the seventh array and for every clock cycle the data is shifted to the above register. After 8 clock cycles the data in the array is forwarded. The SIPO output contains 8 registers of real data and remaining eight imaginary 8 data registers.

4) INVERSE FAST FOURIER TRANSFORM (IFFT): It is the most important module of the OFDM system. The IFFT input will the output from the SIPO. In this system, we require 2 IFFT modules, one for the real and the other for imaginary. The IFFT converts frequency domain constraints to time domain. The time domain values are transmitted as OFDM signals through the transmitter. In this system, IFFT is performed in steps. At first exchange real and imaginary parts, perform FFT, exchange the real and imaginary parts, and finally divide with N, which is the number of inputs fed, here it is 8. At, last we have the time domain values which are transmitted through the transmitter.

B. OFDM RECEIVER BLOCKS

1) FAST FOURIER TRANSFORM (FFT): In the receiver section, this is the main module. OFDM signals are received from the antenna and are fed to the FFT, which converts them back to frequency domain. In this system, Decimation in frequency (DIF)-FFT is used. The Fast Fourier Transform (FFT) transforms a cyclic time domain signal into its equivalent frequency spectrum. This is done by finding the equivalent waveform, generated by a sum of orthogonal sinusoidal components. The amplitude and phase of the sinusoidal components represent the frequency spectrum of the time domain signal.

2) PARALLEL INPUT AND SERIAL OUTPUT (PISO): A parallel to serial converter is a special function of a shift register. The data is loaded parallel into the shift register and then shifted bit by bit. In this system, this bock is used to convert the data obtained from the FFT into serial data and is fed as input to the symbol demapper ,The converter has to wait up to 8 cycles for the next data to be loaded

3) SYMBOL DEMAPPER: Input to this bock is fed from the PISO, from the received real and imaginary parts, based on fixed threshold level, which is of half the amplitude of the input signal, comparing the threshold value with the received input signal, the output is determined. This is the concept behind the QPSK demodulator

4) OUTPUT BIT GENERATOR: This block takes 2 bit IQ from Symbol demapper and generates output bits. This consists of a shift register of 2 bit length, for every clock cycle data is entered, shifted and exited.

III. METHODOLOGY

A simple OFDM system as shown in Fig 1 consists of a transmitter containing serial to parallel converter, QPSK mapper, IFFT block, DAC and a receiver containing ADC, FFT block, QPSK de-mapper and a parallel to serial converter**.**

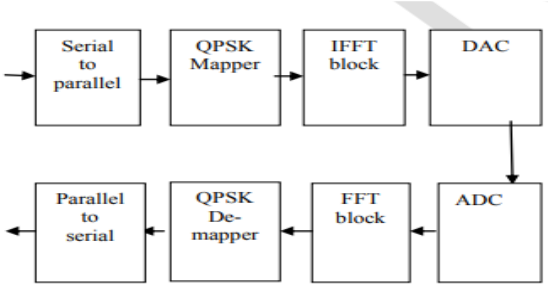

Fig. 1 Proposed Architecture

At first in the receiver part a stream of 8 bits is taken as input and this stream of bits is converted to parallel data. This process is done independently and the VHD file is linked with the rest of the system using structural modeling. The parallel bit stream is then grouped in a pair to map them in the constellation of QPSK. Separate signals are

assigned for processing real and imaginary parts of the mapped signals. A input to output relation is prepared using the butterfly structure algorithm for IFFT calculation. The output of IFFT block is again resolved into real and imaginary parts and separate signals are assigned to them. The input bit pair is checked and accordingly proper equation is synthesized for the output. In the receiver section the output of IFFT block is again processed using the radix-4 butterfly algorithm of FFT. Finally the real and imaginary part of output from the FFT block is de-mapped using the same scheme used in QPSK mapping and corresponding bit pair is thus obtained. These bit pairs are separated and converted to parallel data

CONCLUSION

The main aim of this paper is to implement OFDM systemusing VHDL. The system design flow and associated resultsare discussed in this paper.From the results it can be concluded that the system isworking properly. Also as number of sub carriers increasesthe number of calculations associated with IFFT and FFTalso increases with an increase in spectral efficiency . It was found thatmany blocks need complex multipliers and adders andtherefore special attention needs to be given to optimizethese circuits and maximize reusability. In particular, themodels have been applied to analyze the performance ofmixed-radix FFT architectures used in OFDM. Actualhardware resource requirements were presented andsimulation results were given for the synthesized design.The 48-point Mixed-Radix 8-2 FFT based OFDM architecturewas found to have a good balance between its performanceand its hardware requirements and is therefore suitable foruse in OFDM systemof thissystem.

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