DESIGN AND SIMULATION OF STATUS REGISTER USING MULTIBIT FLIPFLOP FOR UART APPLICATION- (TIME-EC056)

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Abstract:

Universal Asynchronous Receiver and Transmitter (UART) is the microchip for asynchronous serial communication. This paper is mainly focus on the design of status register of UART using multibit flipflop (MBFF) and compares with single bit flipflop (SBFF). MBFF with delay assertion technique is used to reduce the Power and area by merging the flipflops using combination table. While the data is being transmitted as well as received, it will detect some types of errors like parity error, framing error, overrun error and break error. Using the MBFF method the total inverter number is to be reduced by sharing the inverters, it in turns gives reduction of wire length, hence these results in reduction of area and power consumption. The comparison results for the flipflops with merging and without merging by using delay assertion technique are observed.

Keywords -- UART, status register, Multibit flipflop, Delay assertion technique, Quartus II, power play analyser

INTRODUCTION:

One of the transmission data types is serial communication protocol i.e. UART (Universal Asynchronous Transmitter and Receiver). It is mainly used for serial data communication in an asynchronous way and by it converting the data from parallel to serial at the transmitter by adding some extra bits using a shift register.

Synchronizing the flow of data signals among synchronous data paths using clock distribution networks. The network of this design can dramatically affect the reliability and system wide-performance. The skew background is providing a better understanding between the clock distribution networks and interacts with data paths. The timing constraints of high and low clocks are developed from the relative timing between the data paths and localized clock skew network. Reducing the number of switching elements in the circuits internally logical elements and number of flipflops must be reduced.

The process of analysing the timing performance of multi bit flipflop can be done by using simulation in Quartus II and power play analyser as well as tanner tool. Therefore, the results such as clock buffer and gate delays are will be reduced in the clock distribution network. As a result, the total area for the design and power consumption is reduced.

II. UART ARCHITECTURE:

UART architecture or protocol used between the devices in order to communicate. Number of computers and microcontrollers including most of the serial data parts over to connect with other Input as well as output serial devices such as printers, mouse, keyboards. Using a UART can establish a connection between two computers and in each device Serial parts are being used between them. A cross server cable requires establishing a connection between the transmitters of one UART to the receiver other computer UART and vicing versa. In UART communication Transmission of data bit by bit at a time over single data communication cable to the other receiver. To transfer the data over the long distances, this method is useful as it requires low data transfer rates. In serial communication most of the computers consist of one or more serial ports, so it becomes easier than other transmission, hence there is no requirement of hardware. A cable is required in order to establish the connection between the two devices. A UART provides the minimum number of wires to send information. Without giving a clock signal we can send the data bit. The conversion of parallel-to-serial while transmitting and serial-to-parallel when receiving is the Main function of the UART Clock signals. The proposed system of UART comparing it with existing method is explained in this paper.

2.1 LINE CONTROL REGISTER (LCR):

LCR is a Line control register and acts as byte register. The usage of LCR format is to specify the format frame and baud rate decoder. It is used for precise specification of frame format and decided baud rate. By writing the exact bits in LCR we can change the parity bit, baud rate selection, stop bits, wire length.

![Fig: LCR FORMAT](http://www.ijetjournal.org)
2.3 TRANSMITTER SECTION:

The transmitter section receives the parallel data, generates the frame of data and transmits in serial communication and the transmitter output. The FIFO is loaded from TXIN0 - TXIN7. The highest significant bits are not transmitted. When words less than 8 bits are used if least significant bits are transmitted. FI THR (transmitter hold register) will receives the signal from FIFO, if THR is empty then it sends signal to FIFO which gives acknowledgement to THR then it receives the signal from FIFO. THR receive the signal from TSR (transmitter shift register) if it is empty it will send the signal to THR. TSR consist of 12-bit register. The output of TSR consisting of 3 data frames such as data frame bit, stop bit and parity bit. The data is transmitted from TSR to TX OUT serial way.

2.4 STANDARD DATA FORMAT FOR UART:

The frames of 8 data bits and coded information bits are contained in the form of serial data bits. The transmission line should be high during successive transmission. While transmitting the data, transmission is starts by a low start bit first. The 8-bit data frame is transmitted from LSB to MSB after sending the start bit, parity bit is transmitted. these parity bit represents the result of 8 data bits. the parity can be obtained and encoded based on, Weather it seven or odd parity mode. And, at the end of data frame, stop bit is received.

![UART Architecture](image2)

![UART data format](image3)

II. MULTIBIT FLIP FLOP CONCEPT:

The single bit flipflop is shown in figure 3 it has two latches master and slave latch these latches needs the individual clocks so, in order to get better delay, by generating clock from clock. That is, merging of clock pulse.it is called the multibit flipflop concept. figure 5 shows the example of multibit flipflop concept the multibit flipflop contains two inverts, master and slave latch.

![Single-Bit Flip-Flop](image4)

By generating the CLK from CLK can have the better delay from CLK ->Q, so the clock path consists of two inverts. Therefore, it will have two inverts in the clock path. Fig.5 shows an example of combining two one-single flip-flops into one two-bit flip-flop. Each single-bit flip-flop consists of 2 inverters. Master latch and slave latch to store the data in it.
Nowadays, it becomes a trend in emergency to merge flip-flops so that it can reduce the size, power, and other parameters. As the technology advances day by day, the smaller geometrical nodes like 65nm, 85nm, and beyond, the clock drivers have driven more than 1 flip-flop, by the combining or merging one-bit flip-flops into one multi-bit flip-flop, it can avoid the number of replica inverters, and can decrease the total power consumption.

**SIMULATION OUTPUTS:**

- Fig. 1: Simulation results of MBFF
- Fig. 2: Frequency details using MBFF
- Fig. 3: Area analysis using MBFF
- Fig. 4: Power analysis using MBFF
- Fig. 5: Power analysis using SBFF
RESULT ANALYSIS:

By designing the status register using MBFF in UART, the simulated results shown in the MODELSIM, QUARTUS II in POWER PLAY ANALYSER. The power reduction is up to 73.84mW using MBFF whereas power reduced using SBFF is 109.51mW. Therefore 30% of power is reduced using MBFF when compared with SBFF, the simulation results are shown in above figures. Area is reduced in terms by reducing the inverters or the clock buffers using using maximum frequency of about 559.39MHz.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Existing</th>
<th>Proposed</th>
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<tbody>
<tr>
<td>Logic Elements</td>
<td>100</td>
<td>77</td>
</tr>
<tr>
<td>Power</td>
<td>109.51mW</td>
<td>73.84mW</td>
</tr>
<tr>
<td>Dynamic Power</td>
<td>13.04mW</td>
<td>3.12mW</td>
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<tr>
<td>Static Power</td>
<td>18.17mW</td>
<td>18.09mW</td>
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<tr>
<td>I/O Thermal Power</td>
<td>78 mW</td>
<td>52.63mW</td>
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<tr>
<td>$F_{\text{max}}$</td>
<td>420.17MHz</td>
<td>559.39MHz</td>
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</table>

CONCLUSION:

In this paper the VLSI design has addressed one of the most important issues that reducing the utilization of logical parameters. Achieving the experimental results by targeting it into number of clock buffer usage and power consumed by the clock buffer. MBFF has more advantageous over SBFF, and utilizing other reduction techniques can reduce the various parameters.

REFERENCES: