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ULTRA LOW POWER RIPPLE CARRY ADDER USING ADIABATIC TECHNIQUES

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Abstract:

This paper presents the design style and analysis of ultra-low power Ripple Carry Adder using adiabatic families namely ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) logic. These styles have the profit of energy saving as it reuse the certain amount of the energy by recycling from the load capacitance thus reduces the energy dissipation. Simulation is done with the help of T-Spice and analysis is done with the different load capacitance, and different supply voltages. In the investigation it has found that adiabatic is superior for low power applications like Cryptographic hardware for example smart cards, many DSP Processors and embedded systems.

Keywords — ECRL, PFAL, Power clock, low power, Ripple carry adder.

I. INTRODUCTION

The needs of low power in today's market are towering. However, up to date trends towards ultra-low power has prepared VLSI designers for the search of techniques to recover/reprocess from circuits. The energy recovery techniques are now and then called as adiabatic or quasi-adiabatic computing. The "Adiabatic" is a word of Greek basis that designates thermodynamics. It states to a structure in which a switch occurs without energy being either gone to or gained from the structure. And in progress year many adiabatic many adiabatic logic families have been proposed for the low power systems. In this investigation, we have design and simulated the 4-bit Ripple Carry Adder using adiabatic logic families namely ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) logic and compared its power utilization with CMOS ripple carry adder, ECRL RCA is compared with power utilization of PFAL RCA and also analysis is done with the wide range of load capacitance and supply voltage.

This paper has five parts. II part describes the adiabatic logic families namely Efficient Charge Recovery Logic (ECRL) and Positive Feedback Adiabatic Logic (PFAL) while III, IV & V consists of proposed design, analysis and conclusion respectively. Here analysis is done at frequency of 50 KHz. The proposed designs are analyzed at different load capacitance at the constant frequency the constant frequency of 50 KHz and constant load capacitance of 500Ff.

A .CMOS

In CMOS switching, power dissipation occurs mainly due to charging and discharging of load capacitance. During charging half of the energy is charged in to the load capacitance and remaining half of the energy is dissipated through the Pmos arrangement and during discharging remaining of the energy is dissipated through the Nmos arrangement. The total amount of energy drawn from the power supply is $C_L V_{DD}^{2.}$ So full amount of power is degenerate as heat during charging and discharging. Figure.1 shows the CMOS switching and discharging paths followed by both the transistors. In the fig.the basic arrangement of cmos transistors is shown i.e, an inverter circuit using pmos and nmos transistors and load capacitance is connected across the output to charge and discharge.

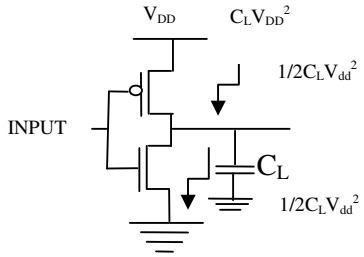


Figure.1. Basic switching analysis in CMOS

B.Adiabatic logic

Energies are preserved rather than dissipating through Nmos and Pmos network in the adiabatic switching at the operating cost of circuit complication. Adiabatic uses power clock it may be single phase or multiple phase depending up on the application and specification.

It reduces the power consumption compared to the CMOS style by using sine or trapezoidal wave form. And also constant current source which is used for recovery of certain amount of energy present in load capacitance. The current stored at the load capacitance is recycled during recovery phase of power clock. Hypothetically, when power clock moves from 0 to V_{DD} the power dissipated in the adiabatic style circuitry will be more or less close to zero. In discharging process power clock is alternated, so the power stored in the load capacitance will be recovered before completely grounded, results in low power requirement for working. It is furthermore called as ENERGY RECOVERY CMOS. This principle state can be achieved by slow switching activity. However dissipation occurs due to the parasitic elements but less than CMOS style. So it also called as quasi adiabatic logic. Figure.2 shows the fundamental charging and recovery process in adiabatic logic devices. As said earlier the energy recovery cmos circuit design is given as below shown in figure with a single pmos transistor showing the power clock and a load capacitor at the output stage to show both charging and discharging process in the circuit design and the pmos transistor is given with Low

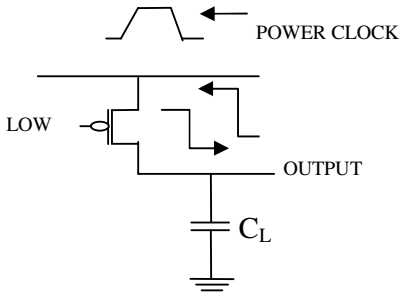


Figure.2. Fundamental charging path and Recovery path in adiabatic sentence gates

II. Adiabatic Families Used In Proposed Designs

Adiabatic logic can be designed in various families that work on different principles of operation. In this paper we have chosen two adiabatic logic styles for the proposed design, they are ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) to implement RCA (Ripple Carry Adder) because of its dependable results in the power consumption reduction and regularly used as an reference for new logic families for evaluating power utilization.

A. Efficient Charge Recovery Logic (ECRL)

In ECRL, two PMOS's are Cross-coupled to grip the position. Power-clock is feed to Source nodes of together PMOS's and gates of apiece transistor are attached to the drain of the further transistor. These nodes form the harmonizing outputs. Set of NMOS switches are used to implement the logic function. This logic family considers four phase clock. Here the pre-charge and the evaluation will be performed in the same time. Hence dissipates less energy than other adiabatic circuits.

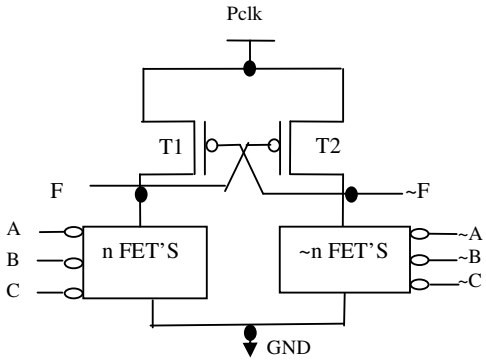


Figure.3. Block Diagram of ECRL

B. Positive Feedback Adiabatic Logic (PFAL)

In PFAL, latches are made by two cross coupled inverters and the logic is implemented with the help of set of NMOS transistors. This methodology also has harmonizing outputs and here logic function is in parallel with the PMOS's so that channel resistance and wire resistance will be small when loads need to be charged. The logic function made of NMOS switch devices is connected between power-clock and the outputs instead of ground and the outputs. During the recovery phase, the NMOS devices between the outputs and the power-clock can provides complete recovery of required outputs. Hence the low-power performance of PFAL can be improved by making it fully reversible. Figure.4. shows the logical structure of PFAL.

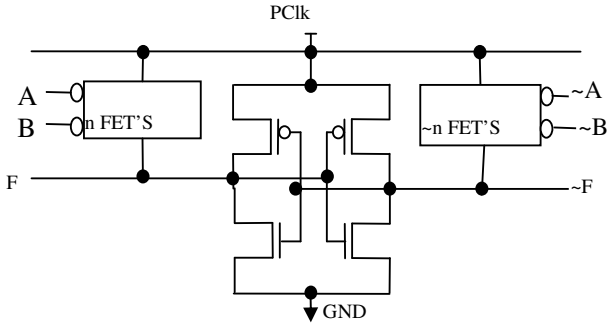


Figure.4. Block Diagram of PFAL

III. Proposed Designs

Adders form the critical part in all digital computation system from small application circuits to microprocessors and Digital Signal Processors. It is important that adders are made to work efficient with respect to its speed and power consumption. As it is known that well that increase in speed may result in increased power consumption, the tradeoff between these must be given a large significance. Since adders become the basic part of most of the computational circuits, the reduction of circuit power utilization with a competitive speed is the every designer's aspiration. In this paper, an energy saving/recovery technique is used to design an ultra low power ripple carry adder (RCA) based on ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) logic families.

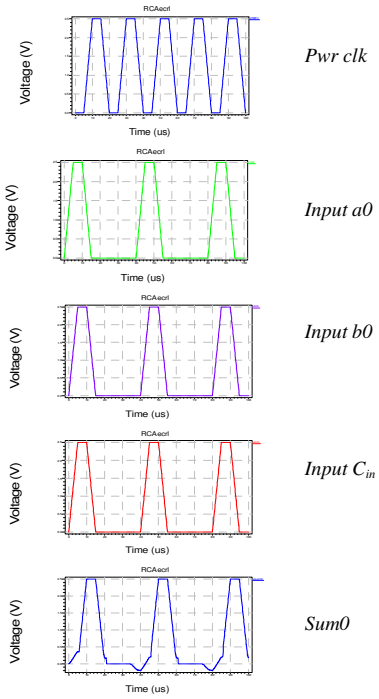
A ripple carry adder (RCA) is used for the addition of binary words, it consist a series of full adders that are provided with two real-time inputs and a carry input. The carry propagates through each stage of adders with a maximum possible computational delay; this makes the final output a delayed data. Stage to stage delay is added to the four phase power clock of each adder's, thus supporting the delayed input. Here the designed ripple carry adder is four bit adder. In ripple carry adder incoming output is calculated only after the arrival of the previous carry out in ripple carry adder.

*A. **Ripple Carry Adder Using Efficient Charge Recovery Logic (ECRL)***

The design of energy recovery logic RCA is made in T-Spice at transistor level uses the model 1102e, where e stands for the electrical model. The block diagram and simulated waveform of ECRL Ripple Carry adder circuit is shown in Figure.5 and Figure.6 respectively. In order to retain the advantage of four phased clocked circuits, the RCA will be implemented with a constant time delay at each stage of the block. All four phases of the clock are equally divided to make the operation provide a proper result. ECRL family operates at low power, with the computations are more dependent on parameters. This makes the circuit beneficial in terms of utilizing/recovering energy at load capacitance. An adiabatic logic reduces the power dissipation at the expenses of complexity of circuit. RCA is used to add the binary words, the design in this paper is four bit ripple carry adder, and it has four full adders. ECRL RCA has the complimentary outputs the simulated waveform shown in Figure 6 shows only one kind of outputs (Sum0, Sum1, Sum2, and Sum3). Its overturned outputs (~Sum0, ~Sum1, ~Sum2, and ~Sum3) are not shown in simulated waveform. The complimentary outputs facilitate to eradicate the inverters, which might otherwise be used. The switching power dissipation of ECRL RCA is low compared to CMOS ripple carry adder.

*B. **Ripple Carry Adder Using Positive Feedback Adiabatic Logic (PFAL)***

The positive feedback adiabatic logic (PFAL), which uses two cross coupled inverters that are powered by four phase clock. This design also utilizes model 1102e of transistors for simulation. The PFAL adder uses more transistors than ECRL design. The simulated waveform and block diagram of PFAL Ripple Carry adder circuit is shown in Figure.7 and Figure.8 respectively Every block provided with a constantly delayed power clock to support the feeding of inputs that are delayed from the previous blocks. So the output of the final block will be at the maximum computation delay. An adiabatic logic reduces the power dissipation at the expenses of complexity of circuit. ECRL RCA has the complimentary outputs the simulated waveform shown in Figure 7 shows only one kind of outputs (Sum0, Sum1, Sum2, Sum3). Its overturned outputs (~Sum0, ~Sum1, ~Sum2, ~Sum3) are not shown in simulated waveform. The complimentary outputs facilitate to eradicate the inverters, which might otherwise be used. The switching power dissipation of PFAL RCA is low compared with CMOS RCA.



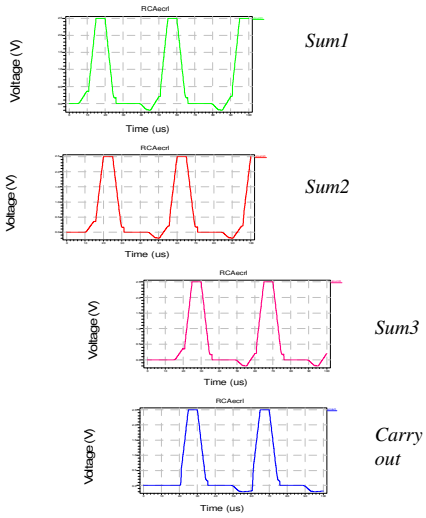
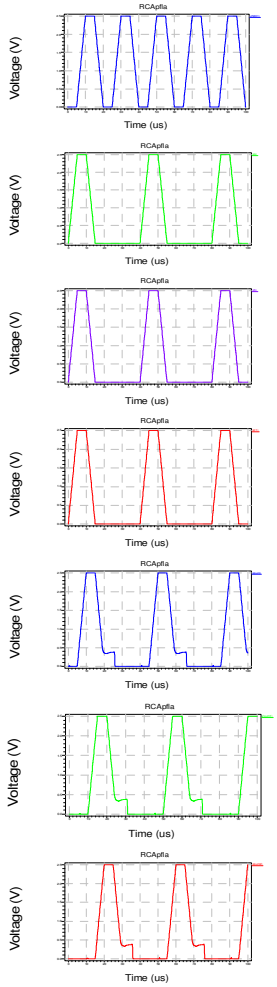


Figure.6. Simulated Waveform of ECRL Ripple Carry Adder Circuit for input 1111+1111 with input carry set to 1.



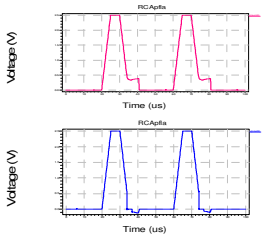


Figure.7. Simulated Waveform of PFAL Ripple Carry Adder Circuit for input 1111+1111 with input carry set to 1.

IV. Investigation with aried loads and supply voltages

ECRL and PFAL adiabatic logic families are extremely needy on parameters .The lessons of power utilization for ECRL CSA and PFAL RCA is done with respect of CMOS RCA circuit with the help of TSPICE simulation, at MOS Level 11 simulation parameters. The following Tabulations provide vital information about the variation in power consumption to change in parameters.

RCA CIRCUIT FAMILY	**NO. of TRANSISTORS**	**POWER ANALYISIS**	
		Load Capacitance (fF)	Power (mW)
CMOS	112	100	0.040565
		200	0.041676
		500	0.041986
PFAL	160	100	0.018253
		200	0.018174
		500	0.017886
ECRL	144	100	0.000135
		200	0.000152
		500	0.000219

Table.1 Power consumed versus Load Capacitance with Frequency kept constant at 50 KHz and Supply voltage at 2.5v

CSA CIRCUIT FAMILY	NO. of TRANSISTORS	POWER ANALYISIS	
		Supply voltage (V)	Power (mW)
CMOS	112	2.0	0.019212
		2.5	0.045654
		3.0	0.067885
PFAL	160	2.0	0.008423
		2.5	0.017886
		3.0	0.032966
ECRL	144	2.0	0.000160
		2.5	0.000219
		3.0	0.000290

Table.3 Power consumed versus change in power clock (supply) voltage with Frequency kept constant at 50 KHz and load capacitance CL=500fF.

V. Conclusion

With the design of Ripple Carry Adder, in two different families of adiabatic logics namely ECRL and PFAL show a considerable improvement in power consumption even with the presence of higher number of transistors. The power analysis table shows clearly that these adiabatic circuits utilize very low power compared to conventional CMOS carry select adder at frequencies ranging in 50 KHz. Change in load capacitance shows a sizable difference in power consumption. Further reduction of power can be made by acting on other parameters of the circuit and including the transistor model also. The stage delay occurring at each stage can be reduced with frequency of operation is also an advantage added with the fast addition operation of the low-power adiabatic ripple carry adder. In our analysis ECRL shows good energy saving than PFAL.

2) *Sanjeeda syed, "deisgn of carry select adder using adiabatic techniques ", in proc. ICEET12.,2012.PP63-67.*

3) *Yadav, R.K.; Rana, A.K.; Chauhan, S.; Ranka, D.; Yadav, K.;"Adiabatic Technique for Energy Efficient Logic Circuits Design", in Proc. ETECT.,2012.,pp.776-780.*

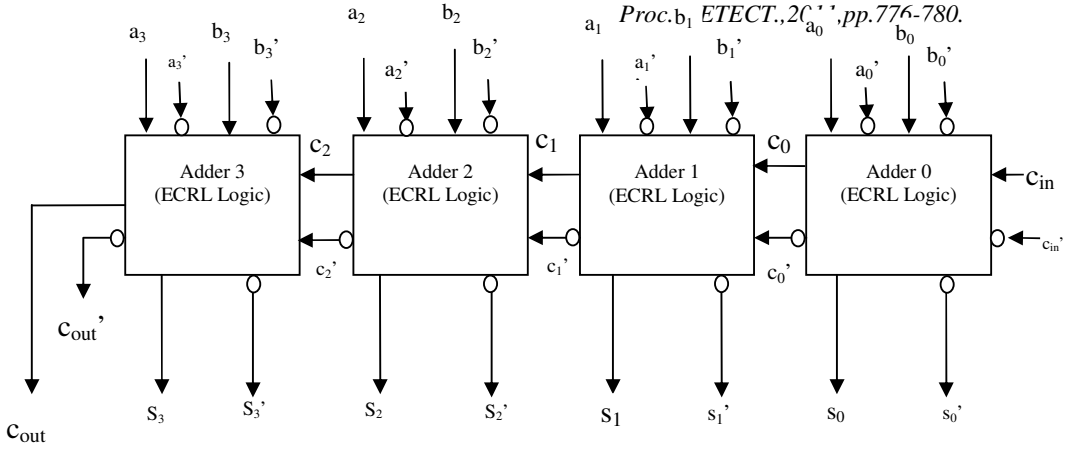


Figure.5 Block diagram of ECRL Ripple carry adder

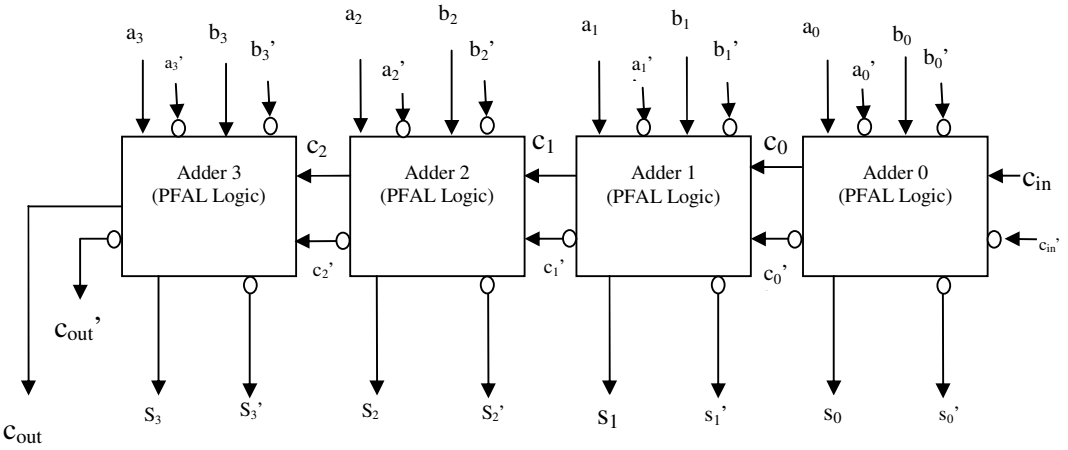


Figure.7Block diagram of PFAL Ripple carry adder

REFERENCES

1) *Pattan vaseem ali khan, G. sambasiva. "design of power efficient digital systems using adiabatic techniques", in IJARECE., JAN 2016 Volume 5, Issue1.*

4) *KEOTE, M. L. and P. T. KARULE. Design*

and Implementation of Energy Efficient Adiabatic ECRL and Basic Gates. In: International Conference on Soft Computing Techniques and Implementations (ICSCTI). Faridabad: IEEE, 2015, pp. 87–91. ISBN 978-1-4673-6792-9. DOI:10.1109/ICSCTI.2015.7489543

5) *DENKER, J. S. A review of adiabatic computing.In: IEEE Symposium on Low Power Electronics.San Diego: IEEE, 1994, pp. 94–97. ISBN 0-7803-1953-2. DOI: 10.1109/LPE.1994.573218*

6) *CALHOUN, B. H., S. KHANNA and R. MANN.Sub-threshold circuit design with shrinkingCMOS devices. In: IEEE International Symposium on Circuits and Systems. Taipei: IEEE,2009, pp. 2541–2544. ISBN 978-1-4244-3827-3.DOI: 10.1109/ISCAS.2009.5118319.*

7) *HEMANTHA, S., A. DHAWAN and K. HARANATH.Multi-threshold CMOS design for lowpower digital circuits. In: IEEE Region 10 ConferenceTENCON. Hyderabad: IEEE, 2008, pp. 1–5. ISBN 978-1-4244-2408-5. DOI: 10.1109/TENCON.2008.4766689.*

8) *MOON, Y. and D. K. JEONG. Efficient chargerecovery logic. In: Symposium on VLSI Circuits,Digest of Technical Papers. Kyoto: IEEE,1995, pp. 129–130. ISBN 0-7800-2599-0. DOI:10.1109/VLSIC.1995.520719.*

9) *KRAMER, A., J. S. DENKER, B. FLOWEand J. MORONEY. 2nd order adiabatic computingwith 2N-2N and 2N-2N2P logic circuits.In: Proceedings of the International Symposiumon Low Power Design. Dana Point: ACM,1995, pp. 191–196. ISBN 0-89791-744-8. DOI:10.1145/224081.224115.*

10) *VETULI, A., S. D. PASCOLI and L. M.REYNERI. Positive feedback in adiabatic logic.Electronic Letters. 1996, vol. 32, iss. 20, pp. 1867–1869. ISSN 0013-5194. DOI: 10.1049/el:19961272.*

11) *BLOTTI, A., S. D. PASCOLI and R. SALETTI.Simple model for positive feedback adiabatic logicpower consumption estimation. Electronic Letters.2000, vol. 36, iss. 2, pp. 116–118. ISSN 0013-5194.DOI: 10.1049/el:20000183.*

12) *YIBIN, Y. and R. KAUSHIK. Ultra Low EnergyComputing using Adiabatic Switching Principle.Purdue e-Pubs [online]. 1995. Available at:* http://docs.lib.purdue.edu/ecetr/114

13) *CHAUDHURI, A., M. SAHA, M. BHOWMIK,S. N. PRADHAN and S. DAS. Implementationof Circuit in Different Adiabatic Logic.In: International Conference on Electronicsand Communication System. Coimbatore: IEEE,2015, pp. 353–359. ISBN 978-1-4799-7225-8. DOI:10.1109/ECS.2015.7124923.*

14) *LIAO, N., X. CUI, K. LIAO, K. MA, D. WU, W.WEI, R. LI and D. YU. Low power adiabatic logicbased on FinFETs. Science China InformationSciences. 2014, vol. 57, iss. 2, pp. 1–13. ISSN1869-1919. DOI: 10.1007/s11432-013-4902-x.*

15) *KUSHAWAHA, S. P. S. and T. N. SASAMAL.Modified Positive Feedback Adiabatic Logic forUltra Low Power VLSI. In: International Conferenceon Computer, Communication and Control.Indore: IEEE, 2015, pp. 1–5. ISBN 978-1-4799-8164-9. DOI: 10.1109/IC4.2015.7375579.*

16) *SHINGHAL, D., A. SAXENA and A. NOOR. AdiabaticLogic Circuits: A retrospective. MIT InternationalJournal of Electronics and CommunicationEngineering. 2013, vol. 3, iss. 2, pp. 108–114.ISSN 2230-7672.*

17) *SINGH, R., A. SHARMA and R. SINGH. PowerEfficient Design of Multiplexer based Compressorusing Adiabatic Logic. International Journalof Computer Applications. 2013, vol. 81, iss. 10,pp. 45–50. ISSN 0975-8887. DOI: 10.5120/14052-2217.*

18) *Y. Moon and D.K. Jeong, "An efficient charge recovery logic circuit,"IEEE J. Solid-State Circuits, vol. 31, no. 4, pp. 514–522, Apr. 1996.*

19) *W. C. Athas, L.J. Svensson, J.G. Koller, N. Tzartzanis, and E. Chou, "Low power digital systems based on adiabatic-switching principles,"IEEE Trans. VLSI Systems, vol. 2, no. 4, pp. 398-407, Dec. 1994*

20) *C. K. Lo and P. C. H. Chan, "An adiabatic differential logic for low-power digital systems," IEEE Trans. Circuits Syst. II, vol. 46, pp.1245–1250, Sept. 1999.*

21) *V.G. Oklobdzija, D. Maksimovic, L. Fengcheng, "Pass-transistor adiabatic logic using single power-clock supply," IEEE Trans. Circ.Syst. II, Vol. 44, pp. 842-846, Oct. 1997*

22) *W. C. Athas, J. G. Koller, and L. J. Svensson, "An energy-efficient CMOS line driver using adiabatic*

switching," Proc. Fourth Great Lakes Symp. VLSI Design, pp. 196-199, Mar. 1994.

23) *T. Indermauer and M. Horowitz, "Evaluation of Charge Recovery Circuits and Adiabatic Switching for Low Power Design," Technical Digest IEEE Sym. Low Power Electronics, San Diego, pp. 102-103,*

.