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14 TRANSISTOR FULL ADDER CIRCUIT USING 4 TRANSISTOR XOR GATE AND TRANSMISSION GATE

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Abstract:

A rapid growth is been observed in the area of Integrated Circuits (IC) technology. All the ICs are to be designed in an optimized way so that they meet all the requirements of being faster, occupying less area and reduced power consumption. One of the circuits which occupy most of ICs is ALU which is a combination of arithmetic and logic units. Of the arithmetic units two are most important which are the adders and multipliers. This paper describes an efficient method to design full adders which is the basic unit of adders in ALUs.

***Key words*: ALU, Logic gates, Pass Transistor Logic, Transmission gate.**

I. INTRODUCTION

Now days all the systems are built on an upcoming technology called System on Chip (SoC) in which all the components and peripherals have been built on a single chip which increases the complexity of the system. VLSI plays an important role in the development of such ideas.

Initially the electronics started their evolution with the invention of vacuum tubes. But with the help of Vacuum tubes only the movement of electrons was studied. After vacuum tubes transistors and diodes were introduced. But for larger circuits it was difficult to fabricate them in a board as they occupied larger space and consumed more power. Also it was difficult for the designers to identify the wiring and routing faults which occurred in such circuits. This led to the invention of Integrated Circuits by Jack and Kilby in which more number of transistors were integrated on a single chip. Initially 3 to 30 transistors were fabricated in a single chip which is known as Small Scale Integration (SSI). Then about 30 to 300 transistors were developed in a single chip which is known as Medium Scale Integration. All the above events happened in 1940S.

Colloquially Moore's law stated that the number of transistors on a single chip doubles each and every eighteen months. Further developments were LSI (300 to 3000 transistors in a single chip), VLSI (3000 to 30000 transistors in a single chip) and now it the upcoming technology is the ULSI with the fabrication of millions of transistors in a single chip. Also Moore's law found a drawback that in even less than eighteen months the number of transistors in a single chip got doubled.

Also circuits were introduced to do the arithmetic and logic operations. Initially logic operations such as AND, OR, NOT, NAND, NOR, EX-OR were done by LSI ICs. And circuits for doing arithmetic operations such as addition subtraction and multiplication were developed which made the field of signal processing and communication field involving arithmetic operations to glow more.

Half adder was designed to add two one bit numbers and when carry arose, that lead to the development of full adders which added three one bit numbers and produced. Full adder acts as the basic block of all adders which are used to perform multi bit additions.

II. Full Adder and its Evolution

A full adder is a logical circuit that performs an addition operation on three one-bit binary numbers. The full adders produce a sum of the two inputs and carry value. It can be combined with other full adders (see below) or work on its own. The full-adder circuit adds three one-bit binary numbers (C A B) and outputs two one-bit binary numbers, a sum (S) and a carry (C1). ... binary numbers. The carry input for the full-adder circuit is from the carry output from the circuit "above" itself in the cascade. The basic full adder circuit is designed from its truth table and its output equations are given by

S= X xor Y xor Z→ (1)

Cout =(X and Y) or (Y and Z) or (Z and X)→(2)

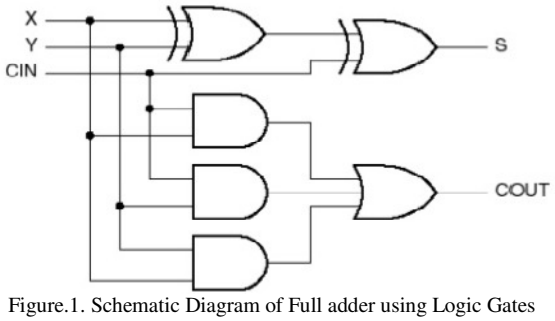

Figure.1. Schematic Diagram of Full adder using Logic Gates

Table.1.Truth Table of Full Adder

X	Y	Z	S	Cout	X	Y	Z	S	Cout
0	0	0	0	0	1	0	0	1	0
0	0	1	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1
0	1	1	0	1	1	1	1	1	1

The above truth table shows the truth table of Full adder and the Schematic Logic Diagram of Full Adder which uses various logic gates. There are also various ways to design the Full Adder circuit in terms of CMOS logic. With increasing demand in speed and power, our main aim is to design Full adder circuit so that it consumes less power and faster. Most of the power in any circuit is being consumed by the power given to the data path of the circuit which consists of the transistors. Hence by reducing the number of transistors we can reduce the power consumption also by reducing the data path, the circuit can be made faster.

III. Static CMOS Logic Style of Full Adder

So many logic styles have been preferred to design CMOS logic circuits. The basic among them is the Static logic which consists of the combination of both NMOS and PMOS. Fig.2, shows the conventional CMOS logic style of representing Full and Pulling down NMOS transistors. The diagram shows that the above logic style uses 28 transistors which in turn lead to high area overhead and high power dissipation

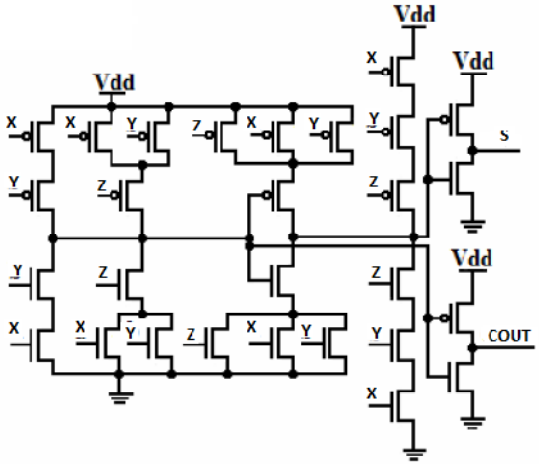

Figure.2. Static CMOS Logic Structure of a Full Adder

IV. Pass Transistor Logic

It is one of the logic styles which use less number of transistors than the Regular CMOS Logic style. In PTL, use of either NMOS or PMOS is enough to send the data. The working of NMOS Pass transistor logic is as follows: Whenever we supply the required gate voltage VG>0.7 V which is the threshold voltage of the transistor, the input message in source is passed on to the drain side as the output. Similarly in PMOS pass transistor logic, when the required gate voltage is VG <-0.7 V, the input data from source is passed on to the drain side. Hence by the above discussed

logic we can reduce the number of transistors used to design a full adder. The main advantage of this logic is that it reduces the area and dynamic power dissipation is reduced. A main disadvantage of PTL is that when the data '0' is passed through the NMOS pass transistor, it is received accurately at the output and when a voltage of 5V is applied as data input to NMOS pass transistor, the output received is 5V-Vth.Similarly it is vice versa for PMOS pass transistor i.e., it passes logic '1' effectively whereas logic 0 is received as 0V- Vth. Hence a new technique called Complementary Pass Transistor logic or the Transmission Gate Logic was introduced. It uses both the NMOS PT and PMOS PT together inorder to send both the data '0' and '1' effectively.

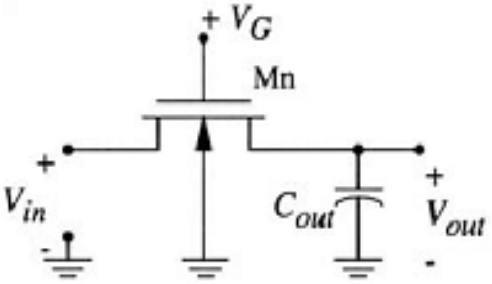

Figure.3a. NMOS Pass Transistor Circuit

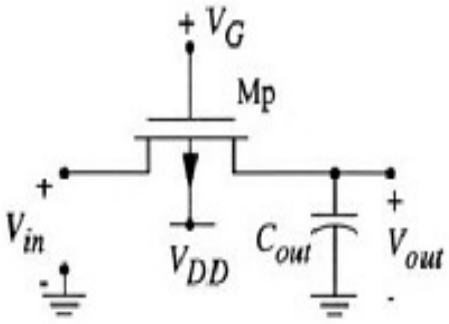

Figure.3b. PMOS Pass Transistor Circuit

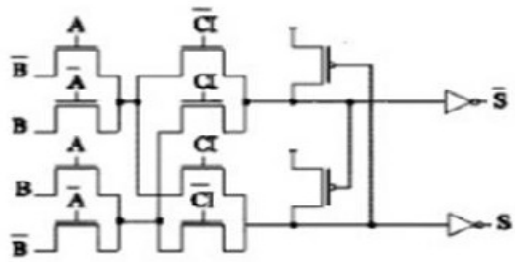

Figure.4a. Logic Circuit For Finding Sum Using Pass Transistor Circuit

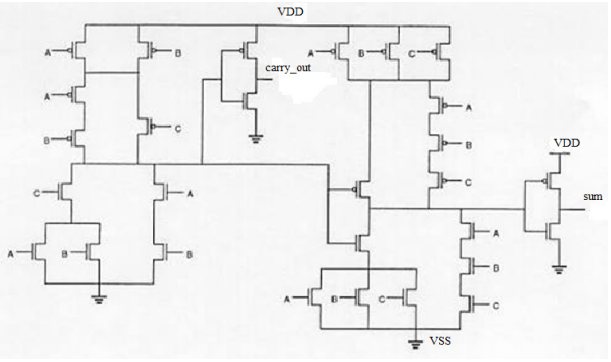

Figure.4b. Logic Circuit For Finding Carry Out Of A Full Adder Using Pass Transistor Logic

V. Transmission Gate Logic

It is another logic style used to design Full adder circuit satisfying requirements such as less delay, less power consumption and reduced Power Delay Product. From the fig.4, it can be seen that Full adders using Transmission Gate Logic uses less number of transistors than Conventional Static CMOS logic and Pass Transistor Logic. The main advantage of using transmission gate design is that it passes both 0s and 1s effectively as follows. When PMOS is off, NMOS is on and it will pass data of logic '1' effectively and reversely when NMOS is off and PMOS is on, it will pass data of logic '0' effectively. Hence this transmission gate logic seems to be an effective method than the previous two methods.

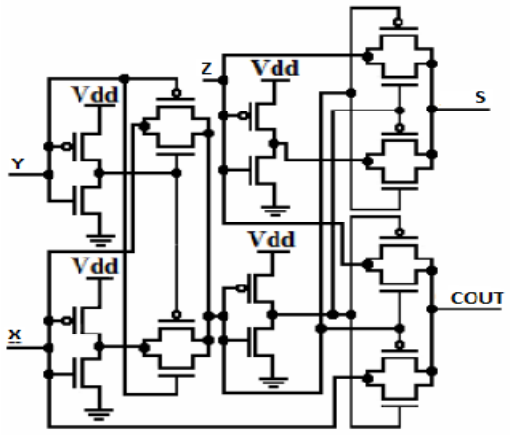

Figure.5. Full Adder Using Transmission Gate Logic

VI. 14T FULL ADDER CIRCUIT

To reduce the number of transistors in the traditional full adder, XOR and XNOR circuits based on the pass transistor logic were used which results in the design of 14T full adder [5] as shown in fig.3. The development of the 14T full adder led to better results for delay as well as power consumption as compared to the previous works in the full adder. 14T full adder worked well with high performance multipliers with less power dissipation. However the adder did not showed improvement in threshold power loss. More over the 14T adder would consume significant power as compared to the presented 28T full adder. The 14T adder with 14 transistors consumes considerably less power in the order of microwatts and has higher speed. The 14T adder reduces threshold loss problem compared to the 28 transistor adders.

In this section single bit full adder circuit is designed by using MOSFET for improve the performance of adder in terms of power and leakage using 14 transistors. This cell is constructed by using the 4T XOR gate. It is the essential element of full adder cell and it generates the basic addition operation of adder cell. It behaves like a single half adder cell. In the 14T full adder cell we used two 4T XOR gate. Conventionally XOR gate use 8 MOSFETs for proper working, but present we have different topologies. Here we have used 4T XOR gate to increase circuit density [11] [12]. Using this XOR gate, reduction in size of full adder is achieved and overall leakage is also reduced. Output waveform of14T full adder is shown in fig.4.The 14T full adder contains a 4T PTL XOR gate, shown in Figure, an inverter and two transmission gates based multiplexer designs for sum and Cout signals[9].This circuit has 4 transistors XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used simultaneously to generate Sum and Cout. It is a faster adder. The circuit is simpler than the conventional adder. The power dissipation in this circuit is more than the 28T adder. However with same power consumption it performs faster [7].

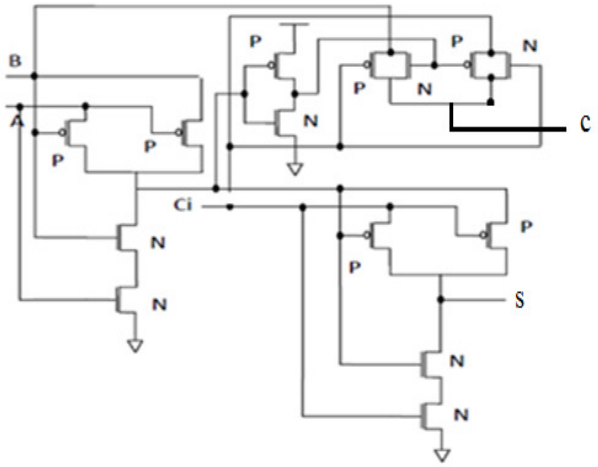

Fig.6(a): Schematic of 14T Full Adder

VII. 4T XOR Gate

The basic element used in the full adder design is the XOR gate which generates basic addition operation in the adder circuits. A single XOR generates simple two bit addition i.e. it behalves like a single half adder. The XOR gate conventionally uses 8 MOSFETs for proper working, however, at present we have different XOR gate topologies [3] [4]. However in this paper, we have used 4T XOR

gate to get proper response and to attain increased circuit density. Figure 4 show the schematic and of 4T XOR gate. Application of this XOR gate would now provide significant reduction in size of full adder thus increasing the circuit density and reducing the overall leakage.

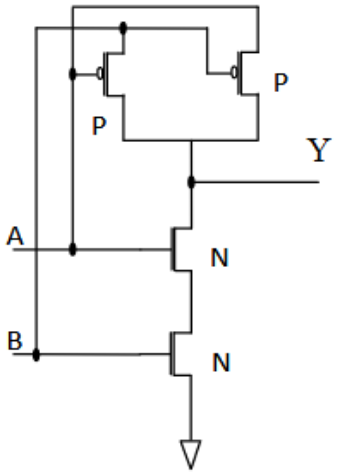

Fig. 6(b): 4T XOR Gate Schematic.

The XOR gate (sometimes EOR gate, or EXOR gate and pronounced as Exclusive OR gate) is a digital logic gate that gives a true (1/HIGH) output when the number of true inputs is odd. An XOR gate implements an exclusive or; that is, a true output results if one, and only one, of the inputs to the gate is true. If either inputs are false (0/LOW) or both are true, a false output results. XOR represents the inequality function, i.e., the output is true if the inputs are not alike otherwise the output is false. A way to remember XOR is "one or the other but not both". XOR can also be viewed as addition modulo 2.

The area evaluation methodology considers all gates to be made up of AND, OR and Inverter (AOI), each having are an equal to 1 unit.

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Table.2.Truth Table of XOR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

If both inputs are false (0/LOW) and both are true, a false output results. XOR represents the inequality function, i.e., the output is true if the inputs are not alike otherwise the output is false. A way to remember XOR is "one or the other but not both".

A way to remember XOR is "one or the other but not both". XOR can also be viewed as addition modulo 2. As a result, XOR gates are used to implement binary addition in computers. A half adder consists of an XOR gate and an AND gate. Other uses include sub tractors, comparators, and controlled inverters.

The 'Exclusive-OR' gate is a circuit which will give a high output if either, but not both, of its two inputs are high. An encircled plus sign (⊕) is used to show the EOR operation. The 'Exclusive-NOR' gate circuit does the opposite to the EOR gate. It will give a low output if either, but not both, of its two inputs are high.

An XOR gate is shown below fig which is implemented by using AND, OR and NOT. The gates between the dotted lines are performing the operations in parallel. The area evaluation methodology considers all gates to be made up of AND, OR and Inverter (AOI), each having are an equal to 1 unit.

Table.1. Comparison of Power for Full Adder Using Different Logics

Type of Logic	No. of transistors used	Power Consumption (µw)
NORMAL PTL	38	39.32
STATIC	28	25.81
PROPOSED 14TR FA	14	3.612

VIII. RESULTS AND DISCUSSION

The above discussed circuits were simulated using the Micro wind DSCH software and the results were obtained. From the simulated results it can be seen that we have less distortion in the proposed 6 TR based full adder using PTL than the above discussed earlier 6 transistor based Full adder. And also we can observe that it shows a remarkable reduction in terms of power consumption and delay also. The comparison o FA design using various logic styles and the measured parameters are shown in Table.1.

IX. CONCLUSION

This paper has given a brief explanation about the different types of logic styles that are used to design VLSI circuits and also we have studied about the design of FA using different logic styles, their pros and cons. Our proposed design has shown a remarkable improvement in delay, area and power whereas less distortion has been observed than the previously designed adders. Further enhancements can be made to reduce these also.

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