RESEARCH ARTICLE OPEN ACCESS

A Reconfigurable FIR Filter Architecture to Trade off Filter Performance for Dynamic Power Consumption

V.Ruth Havila[1], O.Homa Kesav [2], P.Anjaneya[3] , G.K.Rajini[4]

[1]PG Scholar, Dept. Of ECE, AITS, Kadapa, AP,

[2] Research Scholar, school of Electronics Engineering, VIT University, Vellore,

[3] Research Scholar, school of Electronics Engineering, VIT University, Vellore,

[4] Associate Professor, school of Electrical Engineering, VIT University, Vellore,

Abstract:

An architectural approach to design low power reconfigurable finite impulse response (LPRFIR) filter. The LPRFIR is well suited when the filter order is fixed and not changed for particular applications and efficient trade-off between power savings and filter performance can be implemented using the proposed architecture. Generally, FIR filter has large amplitude variations in input data and coefficients. Considering the amplitude of both the filter coefficients and inputs, proposed FIR filter dynamically changes the filter order. Mathematical analysis on power savings and filter performance degradation and its experimental results shows that the proposed approach achieves significant power savings without seriously compromising the filter performance. The power savings is up to 20.5% with minor performance degradation and the area overhead of the proposed scheme is less than 5.3% compared to the conventional approach.

Keywords: Approximate filtering, low power filter, reconfigurable design, high speed filter

1. INTRODUCTION

THE demand for low power digital signal processing (DSP) systems has increased due to explosive growth in mobile computing and portable multimedia applications. One of the most widely used operations performed in DSP is finite impulse response (FIR) filtering. The input-output relationship of the linear time invariant (LTI) FIR filter can be expressed as the following equation:

$$Y(n)=\sum_{k=0}^{N-1} c_k x(n-k) \qquad (1)$$

Where N represents the length of FIR filter, c kthekth coefficient, and x(n – k) the input data at time instant(n-k) . In many applications, in order to achieve high spectral containment and/or noise attenuation, FIR filters with fairly large number of taps are necessary. Many

previous efforts for reducing power consumption of FIR filter generally focus on the optimization of the filter coefficients while maintaining a fixed filter order [1]–[3]. In those approaches, FIR filter structures are simplified to add and shift operations, and minimizing the number of additions/subtractions is one of the main goals of the research. However, one of the drawbacks encountered in those approaches is that once the filter architecture is decided, the coefficients cannot be changed; therefore, those techniques are not applicable to the FIR filter with programmable coefficients. Approximate signal processing techniques [4] are also used for the design of low power digital filters [5], [6]. In [5], filter order dynamically varies according to the stop band energy of the input signal. However, the approach suffers from slow filter-order adaptation time due to energy computations in the feedback mechanism. Previous studies in [6] show that sorting both the data samples and filter coefficients before the convolution operation has a desirable energy-quality characteristic of FIR filter. However, the overhead associated with the real-time sorting of incoming samples is too large. Reconfigurable FIR filter architectures are previously proposed for low power implementations [7]–[9] or to realize various frequency responses using a single filter [10]. For low power architectures, variable input word-length and filter taps [7], different coefficient word-lengths [8], and dynamic reduced signal representation [9] techniques are used. In those works, large overhead is incurred to support reconfigurable schemes such as arbitrary nonzero digit assignment [7] or programmable shift [8]. In this paper, we propose a simple yet efficient low power reconfigurable FIR filter architecture, where the filter order can be dynamically changed depending on the amplitude of both the filter coefficients and the inputs. In other words, when the data sample multiplied to the coefficient is so small as to mitigate the effect of partial sum in FIR filter, the multiplication operation can be simply canceled. The filter performance degradation can be minimized by controlling the error bound as small as the quantization error or signal to noise power ratio (SNR) of given system.

The primary goal of this work is to reduce the dynamic power of the FIR filter, and the main contributions are summarized as follows. 1) A new reconfigurable FIR filter architecture with real-time input and coefficient monitoring circuits is presented.

Since the basic filter structure is not changed, it is applicable to the FIR filter with programmable coefficients or adaptive filters. 2) We provide mathematical analysis of the power saving and filter performance degradation on the proposed approach.

The analysis is verified using experimental results, and it can be used as a guideline to design low power reconfigurable filters. The rest of the paper is organized as follows. In Section II, the basic idea of the proposed reconfigurable filter is described. Section III presents the reconfigurable hardware architecture and circuit techniques used to implement the filter. Discussions on the design considerations and mathematical analysis of the proposed reconfigurable FIR filter are presented in Section IV. Section V shows the numerical results, followed by conclusions in Section VI.

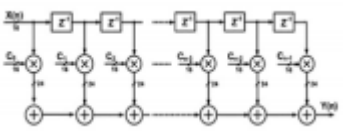

Figure 1: Architecture Of Direct Form FIR Filter

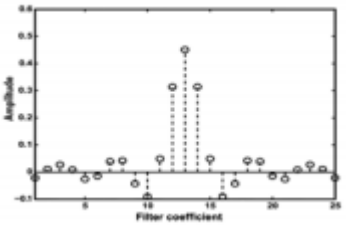

Figure 2: Amplitude Of The 25-Tap Equi-Ripple Filter Coefficient

2. RECONFIGURABLE FIR FILTER TO TRADE OFF FILTER PERFORMANCE AND COMPUTATION ENERGY

As shown in Figure. 1, the weighted values of input sequences sumed up in the FIR Filter operation is known as convolution sum. These are frequently used to implement selection of frequency such as low-pass, high-pass, or bandpass filters. Commonly, the result of summation and its related power of FIR filter are directly proportional to the filter order. The changes of filter order by turning off some of the booth multipliers are done to save the power in it. Even though we save the power, performance degradation should be carefully considered. when we change the filter order. Figure.1.2 exemplary shows the coefficients of a typical 25-tap low-pass FIR filter. The coefficient in centre has the largest value—the coefficient c12 has the largest value in the 25-tap FIR filter and the amplitude of the

coefficients generally decreases as they become more distant from the centre tap. The data inputs of the filter, which are multiplied with the coefficients also have large variations in amplitude. Therefore, the basic idea is that if the amplitudes of both the data input and filter coefficient are small, the multiplication of those two numbers is proportionately small; thus, turning off the booth's multiplier which has negligible effect on the filter performance. For example, since two's complement data format is widely used in the DSP applications, if one or both of the booth's multiplier input has negative value, multiplication of two small values give rise to large switching activities, which is due to the series of 1's in the MSB part. By canceling the multiplication of two small numbers, considerable power savings can be achieved with negligible filter performance degradation. In the fixed point arithmetic of FIR filter, full operand bit widths of the booth's multiplier outputs is not generally used. In other words, as shown in Figure 1, when the bit-widths of data inputs and coefficients are 16, the booth's multiplier generates 32-bit outputs. However, considering the circuit area of the following adders, the LSBs of booth's multipliers outputs are usually truncated or rounded off, (e.g., 24 bits are used in Figure 2) which incurs quantization errors. When we turn off the booth's multiplier in the FIR filter, if we can carefully select the input and coefficient amplitudes such that the multiplication of those two numbers is as small as the quantization error, filter performance degradation can be made negligible .In the following, we denote threshold of input and threshold of coefficient as xthand cth, respectively By threshold, we mean that when the filter input x(n)and coefficient ck are smaller than xth and cth, respectively, the multiplication is canceled in the filtering operation. When we determine xth and cth, the trade-off between filter performance and power savings should be carefully considered.

3. FIR FILTER ARCHITECTURE

In this section, we present a direct form (DF) architecture of the reconfigurable FIR filter, which is shown in Figure. 3 The speed of the filter can be increased significantly, by replacing the conventional multiplier by a booth's multiplier. In order to monitor the amplitudes of input samples and cancel the right multiplication operations, amplitude detector (AD) in Figure 4 is used. When the absolute value of x(n) is smaller than xth the threshold , the output of AD is set to "1".

The design of AD is dependent on the input threshold xth, where the fan in's of AND and OR gate are decided by xth. If it has to be changed adaptively due to designer's considerations, AD can be implemented using a simple comparator. Dynamic power consumption of CMOS logic gates is a strong function of the switching activities on the internal node capacitances. In the proposed reconfigurable filter, if we turn off the booth's multiplier by considering each of the input amplitude only, then, if the amplitude of input x(n) abruptly changes for every cycle, the booth's multiplier will be turned on and off continuously, which incurs considerable switching activities. Booth's multiplier control signal decision window (MCSD) in Figure 3 is used to solve the switching problem. Using ctrl signal generator inside MCSD, the number of input samples consecutively smaller than xth are counted and the booth's multipliers are turned off only when m consecutive input samples are smaller than xth. Here, m means the size of MCSD.

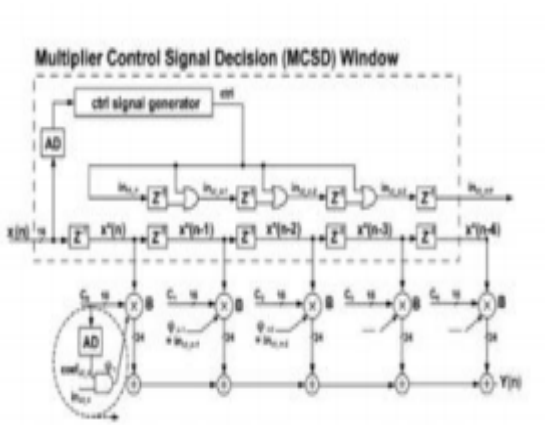

Figure 3: architecture of the reconfigurable FIR filter

Note :ADs and AND gates for each coefficient monitoring are required only in adaptive filter case The above figure shows the ctrl signal generator design. As an input smaller than xth comes in and AD output is set to "1", the counter counts up. When the counter reaches m, the ctrl signal in the figure3.1 changes to "1", which indicates that m consecutive small inputs are monitored and the booth's multipliers are ready to turn off. One additional bit inct_n, in Figure. 3is added and it is controlled by ctrl. The inct_n accompanies with input data all the way in the following flip-flops to indicate that the input sample is smaller than xth and the multiplication can be canceled when the coefficient of the corresponding booth's multiplier is also smaller than cth. inct_n signal is set inside MCSD, the signal does not change outside MCSD and holds

the amplitude information of the input. A delay component is added in front of the first tap for the synchronization between x*(n) in Figure. 4 since one clock latency is needed due to the counter in MCSD. In case of adaptive filters, additional ADs for monitoring the coefficient amplitudes are required as shown in Figure.4 .However, in the FIR filter with fixed or programmable coefficients, since we know the amplitude of coefficients ahead, extra AD modules for coefficient monitoring are not needed, extra AD modules for coefficient monitoring are not needed. When the amplitudes of input and coefficient are smaller than the threshold, the booth's multiplier is turned off by setting signal in Figure 3 to "1". Based on the simple circuit technique [11] in Figure 4 the booth's multiplier can be easily turned off and the output is forced to "0". As shown in the figures, when the control signal is "1", since PMOS turns off and NMOS turns on, the gate output is forced to "0" regardless of input. When is "0", the gate operates like standard gate. Only the first gate of the booth's multiplier is modified and once the is set to "1", there is no switching activity in the following nodes and booth's multiplier output is set to "0". The area overheads of the proposed reconfigurable filter are flip-flops for inct_n signals, AD and ctrl signal generator inside MCSD and the modified gates in Figure 3 for turning off booth's multipliers. Those overheads can be implemented using simple logic gates, and a single AD is needed for monitoring input x(n) as specified in Figure 3 Consequently, the overall circuit overhead for implementing reconfigurable filter is as small as a single booth's multiplier.

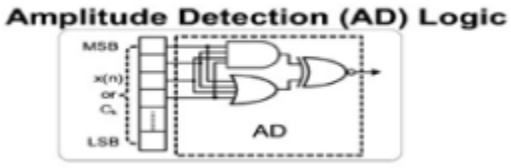

Figure 4: Amplitude Detection Logic(AD)

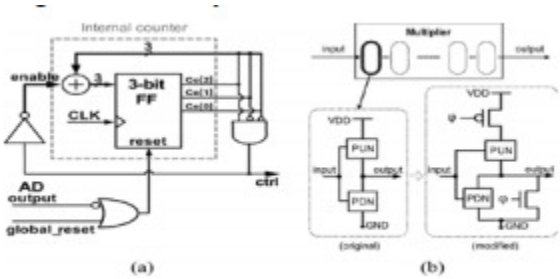

Figure 5(A) Schematic Of Ctrl Signal Generator. Internal Counter Sets Ctrl Signal To "1" When All Input Samples Inside MCSD Are Smaller Than Xth (M= 4 Case).

(B) Modified Gate Schematic To Turn Off Booth's Multiplier.

4. SIMULATION RESULTS

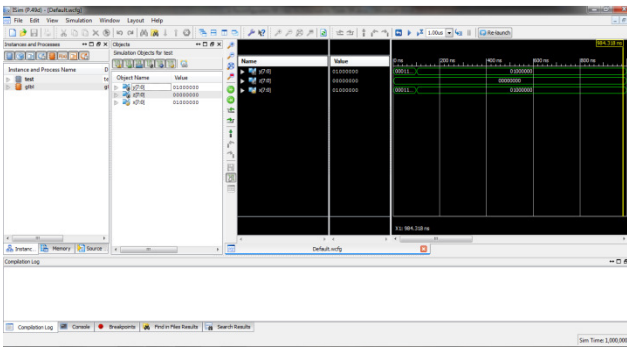

Figure 6: Simulation result for the proposed system

5. CONCLUSION

In this paper, we propose a low power reconfigurable FIR filter architecture to allow efficient trade-off between the filter performance and computation energy. In the proposed reconfigurable filter, the input data are monitored and the booth's multipliers in the filter are turned off when both the coefficients and inputs are small enough to mitigate the effect on the filter output. Therefore, the proposed reconfigurable filter dynamically changes the filter order to achieve significant power savings with minor degradation in performance. According to the mathematical analysis, power savings and filter performance degradation are represented as strong functions of MCSD window size, the input and coefficient thresholds, and input signal characteristics. Numerical results show that the proposed scheme achieves power savings up to 41.9% with less than around 5.34% of area overhead with very graceful degradation in the filter output. The proposed approach can be applicable to other areas of signal processing, where a proper trade-off between power savings and performance degradation should be carefully considered. The idea presented in this paper can assist in the design of FIR filters and its implementation for low power applications.

REFERENCES

[1] H. Samueli, "An improved search algorithm for the design of booth's multiplierless FIR filter with powers-of-two coefficients," IEEE Trans. CircuitsSyst., vol. 36, no. 7, pp. 1044– 1047, Jul. 1989.

[2] R. I. Hartley, "Subexpression sharing in filters using canonical signed digitbooth's multipliers," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 43, no. 10, pp. 677–688, Oct. 1996.

[3] O. Gustafsson, "A difference based adder graph heuristic for multiple constant multiplication problems," in Proc. IEEE Int. Symp. CircuitsSyst., 2007, pp. 1097–1100.

[4] S. H. Nawab, A. V. Oppenheim, A. P. Chandrakasan, J. M. Winograd,and J. T. Ludwig, "Approximate signal processing,"

J. VLSI SignalProcess., vol. 15, no. 1–2, pp. 177–200, Jan. 1997.

[5] J. Ludwig, H. Nawab, and A. P. Chandrakasan, "Low power digital filtering using approximate processing," IEEE J. Solid-State Circuits,vol. 31, no. 3, pp. 395–400, Mar. 1996.

[6] A. Sinha, A. Wang, and A. P. Chandrakasan, "Energy scalable system design," IEEE Trans. Very Large Scale Integr.Syst., vol. 10, no. 2, pp.135–145, Apr. 2002.

[7] K.-H. Chen and T.-D.Chiueh, "A low-power digit-based reconfigurable FIR filter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53,no. 8, pp. 617–621, Dec. 2006.

[8] R. Mahesh and A. P. Vinod, "New reconfigurable architectures for implementing filters with low complexity," IEEE Trans. Comput.-AidedDes.Integr. Circuits Syst., vol. 29, no. 2, pp. 275–288, Feb. 2010.

[9] Z. Yu, M.-L. Yu, K. Azadet, and A. N. Wilson, Jr, "A low power FIR filter design technique using dynamic reduced signal representation,"inProc. Int. Symp. VLSI Tech., Syst., Appl., 2001, pp. 113–116.

[10] R. Mahesh and A. P. Vinod, "Coefficient decimation approach for realizing reconfigurable finite impulse response filters," in Proc. IEEE Int.Symp. Circuits Syst., 2008, pp. 81–84.

[11] J. Park and K. Roy, "A low complexity reconfigurable DCT architecture to trade off image quality for power consumption," J. SignalProcess. Syst., vol. 53, no. 3, pp. 399–410, Dec. 2008.

[12] J. G. Proakis, Digital Communications, 3rd ed. New York: McGraw-Hill, 1995.

[13] Synopsys, Inc., Nanosim Reference Guide, 2007.