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DESIGN OF A POWER EFFICIENT MULTIPLIER USING REVERSIBLE LOGIC GATES

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Abstract:

Reversible computation is emerging region of research, having applications in quantum technology, Nano technology and low power design. It is proved that reversible logic has reduced less power dissipation. This quit different from the conventional logic of multiplication like add and multiplication. The something aspect of the process going that the develop multiplier architecture. Here the design of multiplier by using different logic gates is proposed. The proposed reversible multiplier is implemented using mentor graphics tools in 130 nm technology is very power efficient. Here power dissipation of proposed multiplier design and conventional multiplier has been compared. Conventional multiplier dissipates the power 50.55nWatts where as proposed multiplier designs dissipate 30.33nWatts respectively.

I.INTRODUCTION

Now- days the main requirements for VLSI chip that are hidden to be kept. The three most important methods to measure the quality of VLSI circuits is the area, power dissipation and high speed. The common multiplication method is add and shift algorithms. The main Para meter that determines the performance of the multiplier. The design of multiplier is based on equally distant from one another at all points. A logic synthesis technique using a reversible gate should have the features like minimum gate count along with to smaller extent uses of constant and garbage generation. In next section we will converseassorted operation. Another multiplier it reduce the less power and it change to the different operations of the in filtering process also we have multiplication.

II.REVERSIBLE LOGIC:

The reversible logic is promising computing design paradigm which presents method for constructing computers that produce no heat dissipation. Reversible computing emerging as a consequence of the meaning of quantum mechanics principles towards the developments of a universal computing are based on the connection between entropy. The basic principle of reversible computing is that a bi-ejective device with identical number of input and output lines will produce computing environment where electrodynamics of the system.The total amount of something refers to the cost the moving around in terms of the orbit of primitive gate.

III.PROPOSED WORK FOR 4*4 REVERSIBLE GATES:

Number of computations required to perform the same operation. The proposed one through reversible architecture performs all these operations as mentioned among these the multiplication and accumulation operation .By using this multiplier we have reduced the power consumption to maximum extent by reducing the number of computations required.It not only helps us to determine the output from the input but also helps us to uniquely recover the inputs from the outputs.

A	B	C	D	P	Q	R	S
'0'	'0'	'0'	'0'	'0'	'0'	'0'	'0'
'0'	'0'	'0'	'1'	'0'	'0'	'1'	'0'
'0'	'0'	'1'	'0'	'0'	'1'	'1'	'1'
'0'	'0'	'1'	'1'	'0'	'1'	'0'	'0'
;0;	'1'	'0'	'0'	'0'	'1'	'1'	'0'
'0'	'1'	'0'	'1'	'0'	'1'	'0'	'1'
'0'	'1'	'1'	'0'	'1'	'0'	'0'	'1'
'0'	'1'	'1'	'1'	'1'	'0'	'1'	'1'
'1'	'0'	'0'	'0'	'1'	'1'	'1'	'0'
'1'	'0'	'0'	'1'	'1'	'1'	'0'	'1'
'1'	'0'	'1'	'0'	'1'	'1'	'0'	'1'
'1'	'0'	'1'	'1'	'1'	'1'	'0'	'0'
'1'	'1'	'0'	'0'	'1'	'0'	'1'	'1'
'1'	'1'	'0'	'1'	'1'	'0	'1'	'1'
'1'	'1'	'1'	'0'	'1'	'0	'0'	'0'
'1'	'1'	'1'	'1'	'1'	'0'	'1'	'0'

TABLE 1: Truth table of TSG gate

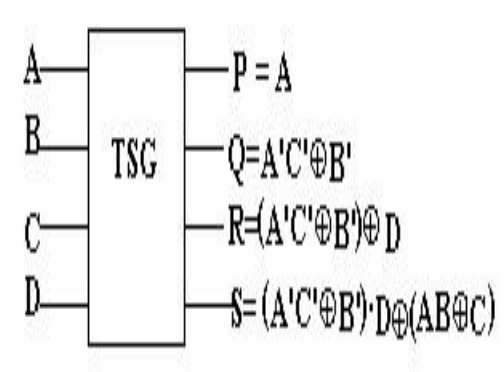

Fig 1: proposed tsg gate.

CMOS IMPLEMENTATION OF TSG GATE.

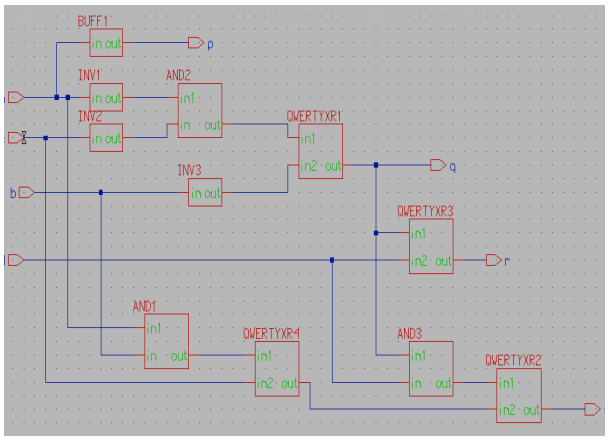

Fig 4: CMOS implementation of TSG gate.

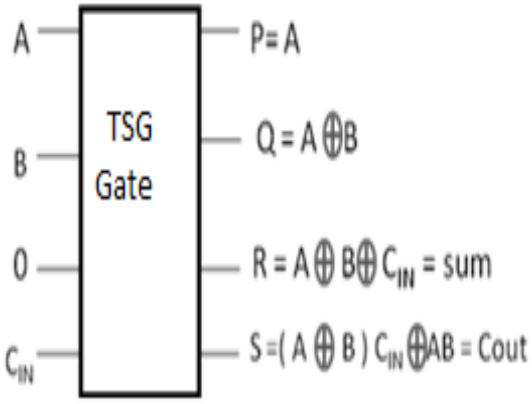

Fig 2: TSG gate implemented as a full adder.

IV. REVERSIBLE MULTIPLIER ARCHITECTURE:

The process of computing the sum of a number with self a specified number of times .The amount of circuitry involved is directly proportional to the square of its resolution. A multiplier of size n bits has n2 gates.Partial products will be added to the reversible parallel adder. The conventional array multiplier uses carry save adder to add the products .The first row of the partial products is implemented with full adder, C in will be considered 0.

That's why if one also aims to minimize power consumption, it is of great interest to reduce the delay by using various delay optimizations .In the 4*4 multiplier, it easy prove correctness, but it's not obvious that it is also totally correct.

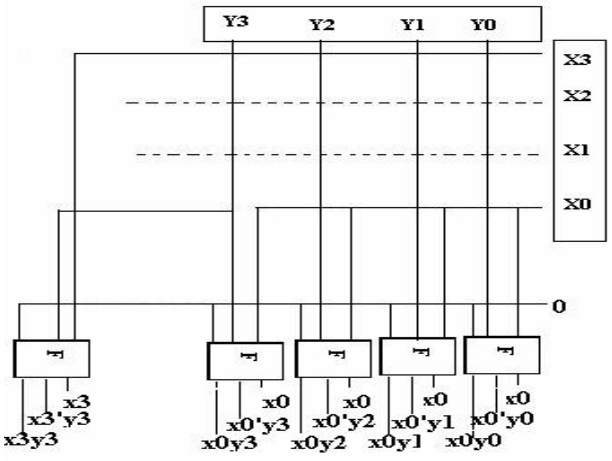

Fig 3. Partial products using fredkin gates.

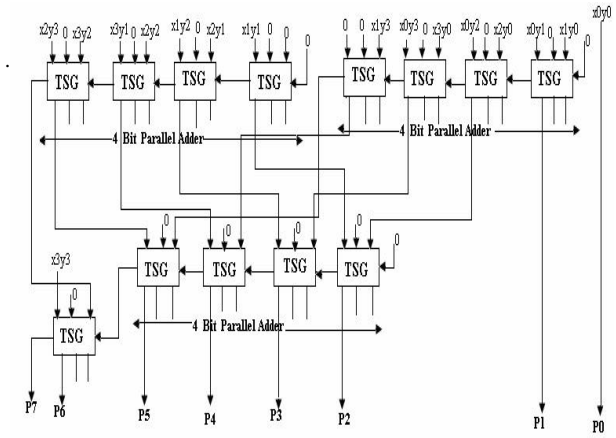

Fig 5: proposed 4*4 reversible multiplier.

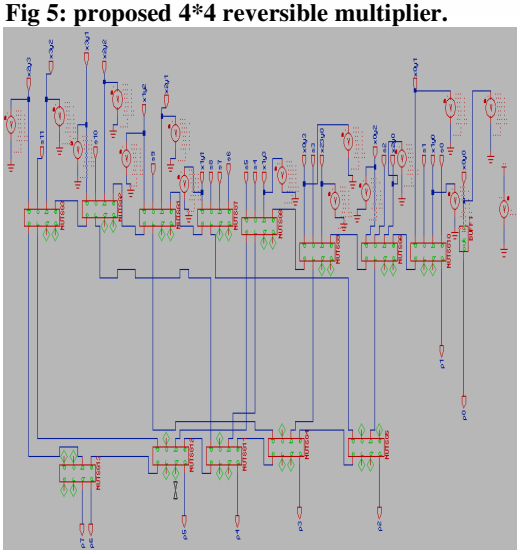

Fig 6: CMOS implementation of 4*4 reversible multiplier.

V.COMPARSION RESULTS:

Here all the reversible logic gates are simulated by using mentor graphics tool with 130 nm technology. Also here were comparing the parameters like power dissipation, delay and slew rate for all the reversible logic gates .The simulation results for TSG gate can be obtained by mentor graphics is shown in fig 6.

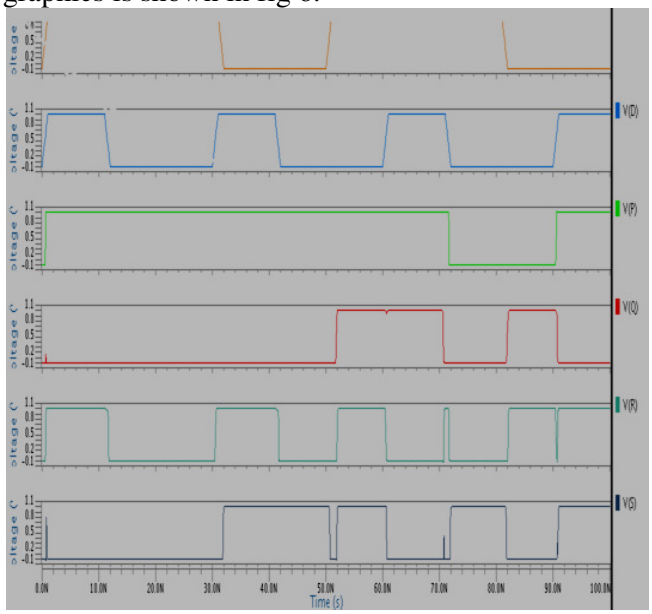

Fig 7: Simulation waveforms for TSG gate.

The Simulation results for proposed TSG gate can be obtained by mentor graphics is shown in fig 7.

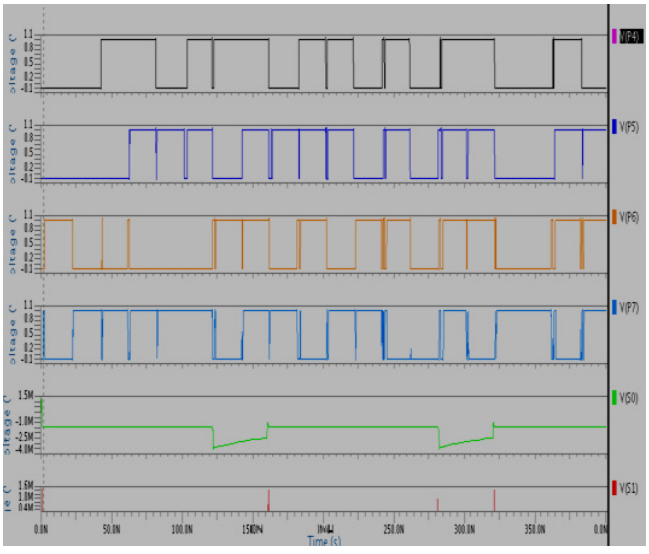

Fig 8: Simulation waveforms for proposed TSG gate.

The comparison of parameters of reversible logic gates is shown in below table.

Parameters	Existing Circuit	Proposed Circuit
Power dissipation	50.55nWatts	30.31nWatts
Delay	60.33NS	40.31NS
Slew Rate	15G	10G

VI.CONCLUSION:

This research work is about efficient reversible realization of the proposed reversible 4*4 TSG gate. Here both conventional and proposed multiplier design can be implemented by using Mentor Graphics tool. The proposed multiplier designs dissipate less power than the conventional multiplier. The total power dissipation for conventional multiplier is 50.55nWatts where as the proposed multiplier design has 30.33nWatts respectively. This project in future extended to more bits.

VII. ACKNOWLEDGEMENT:

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