Analog Layout Design and Analysis for DAC in 28nm Technology

M.Hanumanth Guide[1], S.Vani[2], N.Vanajeswari[3],K.Sudheer Reddy[4]

1. (Department of ECE, Annamacharya Institute of Technology & Sciences, Rajampet Email.com: mhanumanth@gmail.com)

2. (Department of ECE, Annamacharya Institute of Technology & Sciences, Rajampet Email.com: vanichinni212@gmail.com)

3. (Department of ECE, Annamacharya Institute of Technology & Sciences, Rajampet Email.com: vanajanandyalac5@gmail.com)

Abstract: **In order to meet the stringent performance requirements and endless applications, almost all electronic devices are equipped with the DACs. Digital to analog conversion is a process of transforming a discrete signal into a corresponding continuous signal .in modern era, chip design is one of the methodology to have high speed, less power consumption, effective use of space, easily available productivity and mobility with the fast advancement of CMOS 28nm technology, more and more signal processing functions are implemented in the digital domain for low cost, low power consumption, higher yield and higher reconfigurability.**

Keywords**: digital to analog converters, operational amplifier, CMOS.**

I. INTRODUCTION:

Digital to analog convertor (DAC) There square measure many DAC architectures; the quality of a DAC for a selected application is set by figures of advantage including: resolution, most oftenness et al. Digital-to-analog conversion will degrade a symbol, therefore a DAC ought to be such that that has insignificant errors in terms of the appliance.

DACs square measure usually utilized in music players to convert digital information streams into analog audio signals. they're conjointly utilized in televisions and mobile phones to convert digital video information into analog video signals that hook up with the screen drivers to show monochrome or color pictures. These 2 applications use DACs at opposite ends of the frequency/resolution trade-off. The audio DAC may be a low-frequency, high-resolution sort whereas the video DAC may

be a high-frequency low- to medium-resolution sort.

Due to the complexness and also the want for exactly matched elements, well-nigh the foremost specialised DACs square measure enforced as integrated circuits (ICs)

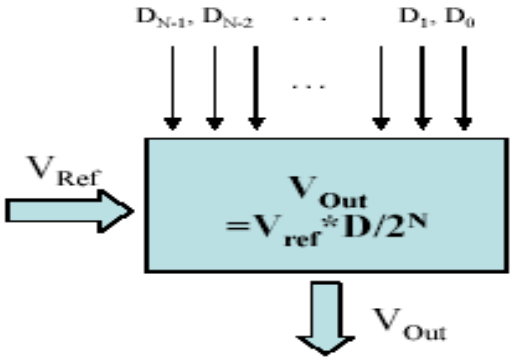


Fig: digital to analog converter

II. CLASSIFICATION OF DAC:

DACs have a wide range of classification. There are different types of DAC. The main converter topologies are: R-2R ladder DAC, binary weighted resister.

A. BINARY WEIGHTED RESISTOR:

It consists of a transistor switch which turns on the switch when the digital input is '1' and if digital input becomes '0' it will open the switch. When transistor switch gets closed, current flows through the weighted resistor due to the reference voltage as shown in circuit diagram.

When all such currents from different weighted resistors get added at summing point of the operational amplifier it will produce a proportional voltage as its output.

For a 4 bit DAC, the output V0 is given as follows

$$V_o = -V_{ref}\left(S_3 \times \frac{Rf}{R3} + S_2 \times \frac{Rf}{R2} + S_1 \times \frac{Rf}{R1} + S_0 \times \frac{Rf}{R0}\right)$$

Where S3,S2,S1andS0 represents the status of the switches i.e. on or off (1 or 0).

If resistors are in binary weights i.e. R3=2Rf, R2=4Rf, R1=8Rf and R0=16Rf, the above equation can be written as,

$$V_o = -V_{ref}\left(\frac{S3}{2^1} + \frac{S2}{2^2} + \frac{S1}{2^3} + \frac{S0}{2^4}\right)$$

From the above discussion, we can say that for a 4 bit DAC 4 switches produces 16 different combinations of output and hence produces 16 different output voltage . in general n-bit DAC produces 2^n different discrete analog voltages.

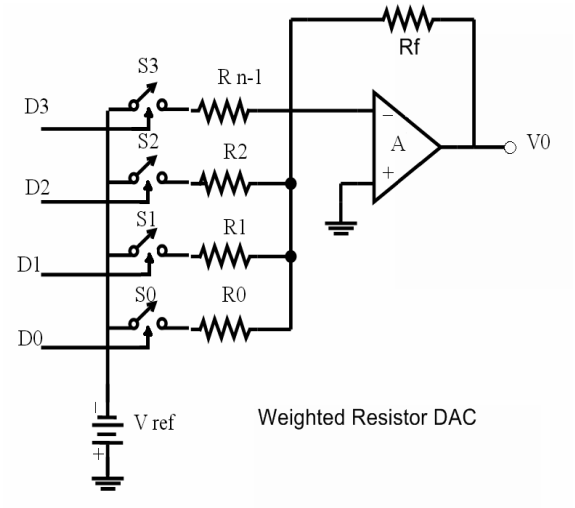


Fig: weighted resistor DAC

B. R-2R LADDER RESISTOR DAC:

An enhancement of the binary-weighted resistor DAC is the R-2R ladder network. This type of DAC utilizes Thevenin's theorem in arriving at the desired output voltages. The R-2R network consists of resistors with only two values - R and 2xR. If each input is supplied

either 0 volts or reference voltage, the output voltage will be an analog equivalent of the binary value of the three bits. VS2 corresponds to the most significant bit (MSB) while VS0 corresponds to the least significant bit (LSB).

Vout =-(VMSB+Vn+VLSB) = - (VRef + VRef/2 + VRef/ 4)

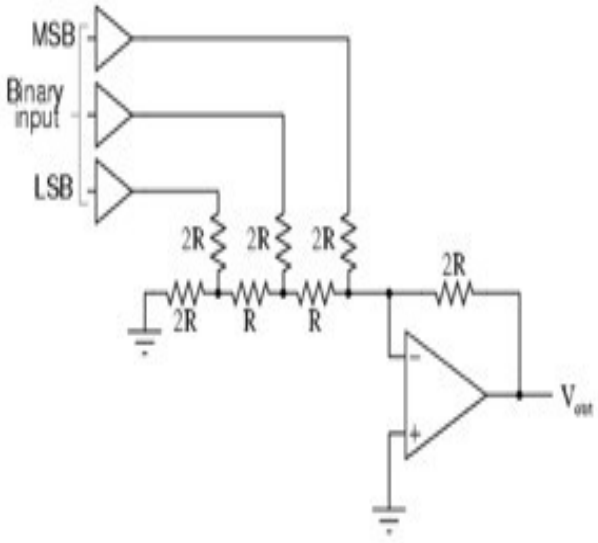
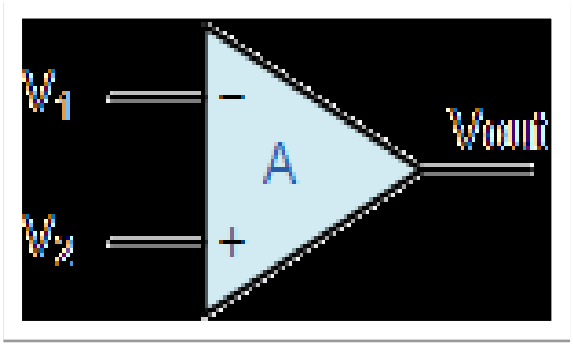


Fig: R-2R ladder resistor

III. OPERATIONAL AMPLIFIERS:

Operational amplifiers square measure linear devices that have all the properties needed for nearly ideal DC amplification and square measure thus used extensively in signal learning, filtering or to perform mathematical operations like add, subtract, integration and differentiation.

The amplifier's differential inputs accommodates a non-inverting input (+) with voltage V+ associated an inverting input (–) with voltage V−; ideally the op-amp amplifies solely the distinction in voltage between the 2, that is named the differential input voltage. The output



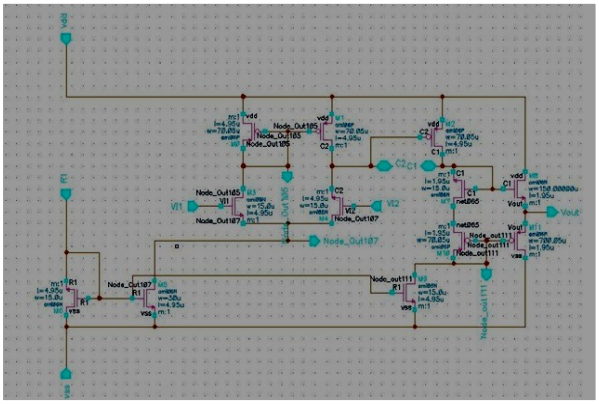


Fig: schematic diagram of operational amplifier

It mainly consists of two blocks

1. Differential pair
2. Current mirror

C. Differential pair:

using MOSFET's is shown below

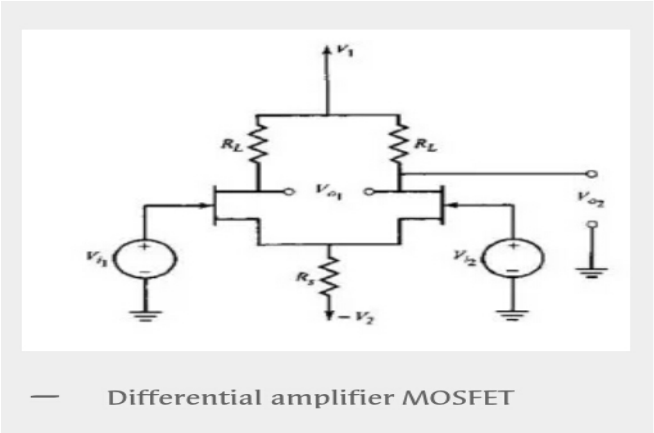


Fig: differential amplifier

The differential amplifier is probably the most widely used circuit building block in analog integrated circuits Differential amplifiers are used to amplify analog as well as digital signals It can be used in various implementations to provide an output from the amplifier in response to differential inputs.

Why it is used:

- ❖ Better common mode noise rejection.
- ❖ Reduced harmonic distortion.
- ❖ Increased output voltage swing.

D. Current mirror:

is often operational in saturation region as its gates and drain terminals are shorted. As Q1& Q2 have common gate, their gate to supply voltages Vdd are identical and therefore the current through Q1 and Q2 should be equal if their dimensions are identical .The currents in 2 transistors are reflected thus it's named as current mirror

In this circuit Q1 act as a supply device and also the remaining devices are mirrored devices .in current mirror the output of supply device is connected to input of the opposite devices.

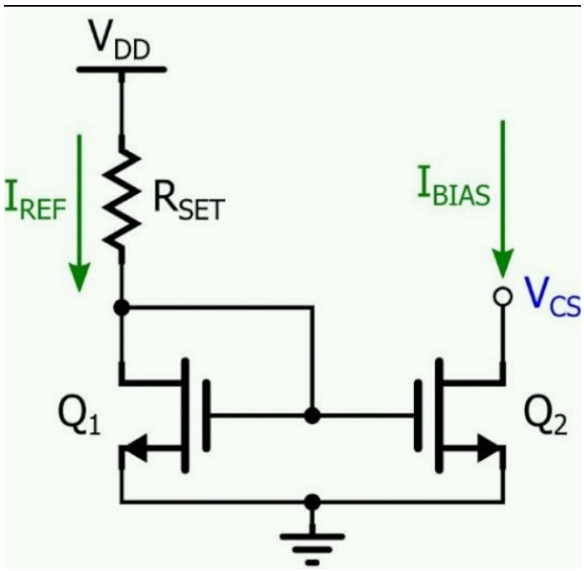


Fig: current mirror

IV. MATCHING CONCEPT:

Analog circuits usually use structures like differential amplifiers and current mirrors ,matching of device characteristics ar vital like threshold voltage.

Matching ideas ar of 2 sorts. They are:

1. Inter digitization matching
2. Cross coupled matching

E. Inter digitization matching:

For current mirror one in all the common matching technique called inter digitization is employed. during this case 2 devices to be matched are split into many fingers and placed during a pattern. as a result of finish components have totally different boundary conditions, dummy devices are usually additional at the tip of the rows to additional cut back matched effects.

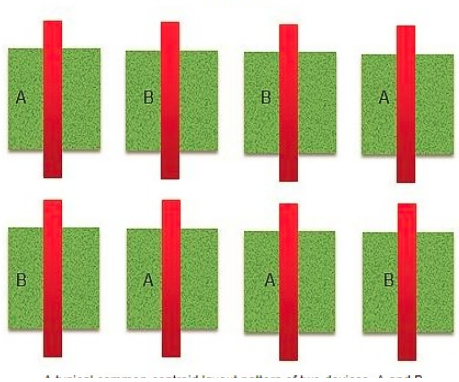


Fig:inter digitization

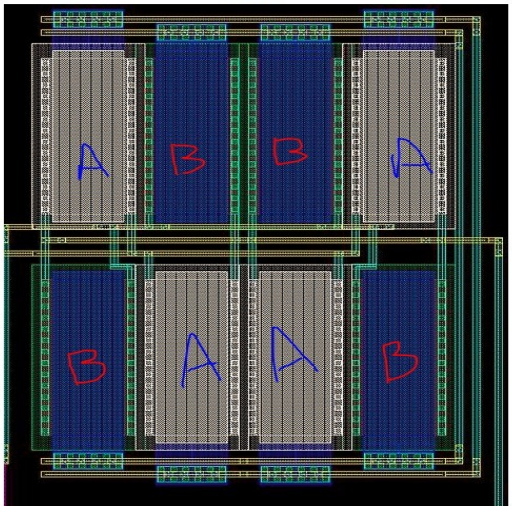
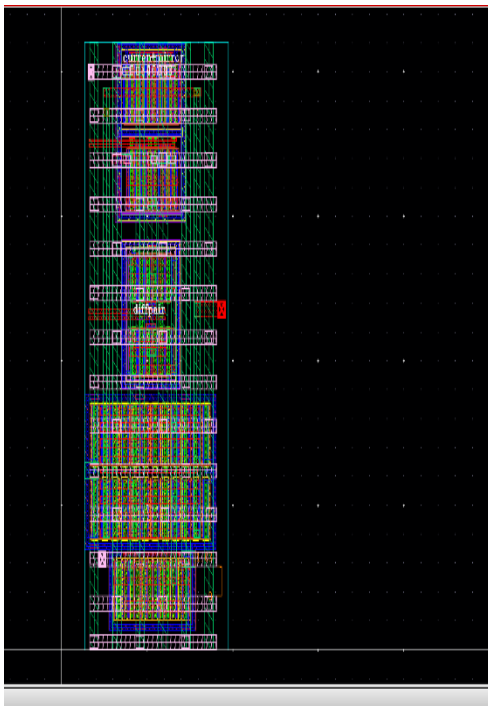
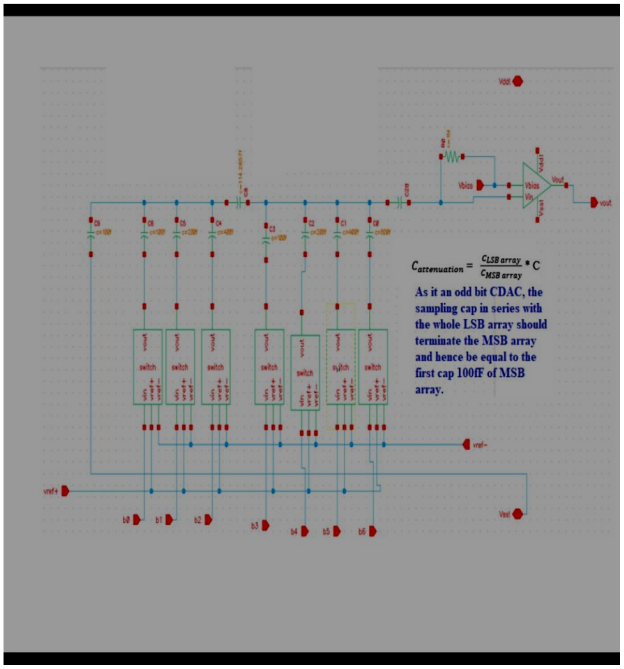


Fig:layout of inter digitization

E. OP -AMP LAYOUT:



F. Schematic of R-2R DAC:



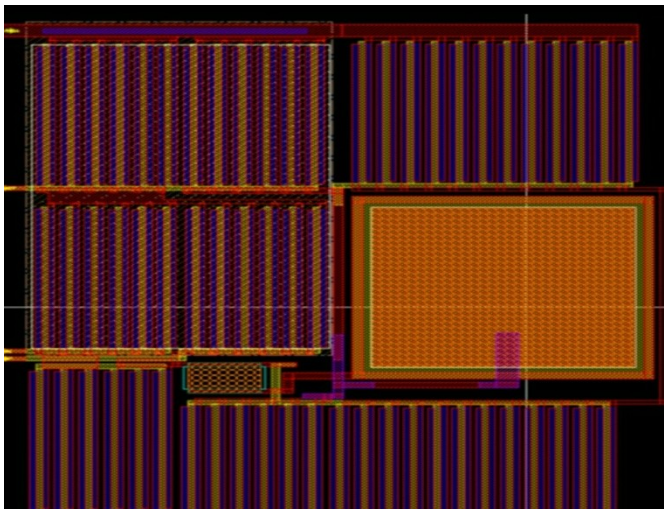


Fig :layout of R-2R DAC

DAC parameters like power consumption, area, delay and has been calculated as shown in

TABLE I

DAC PARAMETERS

Parameters	180	28
Technology(µm)	0.180	0.28
Supply voltage(v)	1.8	0.8
Power consumption(mW)	48.6	27.04
Area(mm^2)	0.054	
Resolution(bits)	8	8

V. CONCLUSIONS:

A 8-bit R-2R DAC is designed and implemented in cadence virtuoso tool using 28nm CMOS process. This DAC is designed for low power consumption, low active chip area, and low DNL. As compared to previous work in 28nm technology, power is reduced from 48.6 to 27.04mW and DNL is reduced from 0.6 to 0.03. Comparing from 130nm technology, DNL is reduced from 0.7 to 0.03 and active chip area is reduced from 0.072 to 0.054mm

VI. REFERENCES

[1] Tutorial: Digital to Analog Conversion The R-2R DAC, Alan Wolke, May 2013.

[2] Anshul Agarwal, Design of Low Power 8-Bit Digital-to-Analog Converter with Good Voltage-Stability, Center for VLSI and Embedded System Technologies International Institute of Information Technology Hyderabad, India May 2013.

[3] Arpit Kumar Baranwal, "Design and Analysis of 8 Bit Fully Segmented Digital to Analog Converter" IEEE 2nd International Conference on Recent Advances in Engineering & Computational Sciences (RAECS), Dec 2015

. [4] Hong Liu; Ning Tang; Mingliang Wang; Zhao Xia; Ke Zhang; Tian Tong"A Monolithic 12-Bit Digitally CalibratedD/A Converter" IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS), Dec 2013, pp. 449-452.

[5] Hicham Akhamal, Hassan Qjidaa, "A low power 6-bit current-steering DAC in 0.18-µm CMOS process" IEEE Intelligent Systems and Computer Vision (ISCV), 2015, pp. 1-5

[6] Aiman Abdullah Noorwali; Syed Manzoor Qasim; Ahmad Samim Doost; Anh Huynh, "A 16-bit 4 MSPS DAC for lock-in amplifier in 65nm CMOS" IEEE 13th International Conference on Networking, Sensing, and Control (ICNSC), April 28-30, 2016, pp. 1-6

[7] Rudy J Van de Plassche. CMOS integrated analog-to-digital and digital-to-analog converters, volume 2. Kluwer Academic Publishers Dordrecht, 2003.

[8] C. Joo, S. Kim, K. Yoon, "A low-Power 12-Bit 80MHz CMOS DAC Using Pseudo-Segmentation",GLSVLSI 2008, May 2008, pp. 219-222

[9] Guoyuan Fu, H. Alan Mantooth, and Jia Di, "A 12-Bit CMOS Current Steering D/A Converter with a Fully Differential Voltage Output" IEEE, May 2011.

[10] B.Razavi, —Design of Analog CMOS Integrated Circuits, New York: Mc-Graw Hill ,2001.

[11]] D. Johns and Ken Martin —Analog Integrated Circuit Design, Wiley India Pvt. Ltd, 1997

[12] Kang Sung-Mo, Leblebici Yusuf, - Cmos digital integrated circuits, analysis and design (Tata McGraw-Hill Edition 2003, Third Edition).

[13] P. Allen and D. Holberg, CMOS Analog Circuit Design. New York: Holt Rinehart and Winston, 1987.

[14] Sonu kumar, Anjali sharma, Payal jangra, Pooja Rathee, Rekha yadav, "Design of CMOS operational amplifier in 180nm technology", Volume5, Issue4, April2017, doi:10.15680/IJIRCCE.2017.0504001.

Q1

IV.