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Relative Analysis of 32 Bit Ripple Carry Adder and Carry Lookahead Adder

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Abstract:

Adders acts as a crucial part in the digital signalling systems. The design of 64 –bit adders is of high importance because 64 –bit architecture is common and hugely used in most of the digital systems and processors.in this paper the theme is to design and implement various 64-bit adders like Ripple Carry Adder(RCA),Carry look ahead Adder(CLA).for different full adder cells is done using VHDL .The simulation and implementation results are obtained by executing VHDL code in Xilinx 14.5 ISE Design suite.

Keywords:Carry look ahead adder, Ripple Carry adder,CLA,RCA,VHDL,Full adder.

Introduction:

In this paper we mainly focus on 32- bit ripple carry adder and carry look ahead adder.Namely there two types of adders, like serial adder and parallel adder.in a parallel adder ,the length n of augend and the addend with the input carry of LSB are available in registers and given as inputs to the respective adders. This is a faster than serial adder. The speed is attenuated by time needed for the carry produced, propagates to stages upto MSB.Hence the name Ripple is acquired.The speed of a adder is reduced by the time.That much time should be given for the outputs to settle before the inputs vary.The output carry ina certain stage of adder completely depends on the augend and addend of the last stage. Holding the argument until the final stag (n-1) stage. In

ripple carry adder there is much dependency of output.Hence there exsists a delay.This needs the carries that could be generated or propagated through the stages from LSB to MSB.This requirement could be achieved through another adder called "Carry look ahead adder" or "Fast adder". The layout of ripple carry adder is simple, which allows for fast design time however,RCA is relatively slow,since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can be easily calculated by inspecting the full adder circuit,each full adder requires three levels of logic.In a 32 bit RCA,there are 32 full adders, so the

critical path (extreme case) delay is 31*2 (for propagating carry)+3(for sum)=65 delays of gate.

A carry-look aheadadder (CLA) or fast adder is a form of adder in digital logic design.CLA improvises the speed by limiting the time needed to calculate carry bits.It could differ with the simple,but slower,RCA for which the carry bit is calculated alongside the sum bit,and each bit should wait till the previous carry bit have been determined to begin calculating its own output and carry bits.The CLA calculates one or more carry bits before the sum,which limits the delay time to calculate the result of the larger value bits of the adder.The kogge-stone adder and Brent-kung adder are theexamples of this type of adder.Carrylookahead logic uses the concepts of generating and propagating carriers.Although in the factors of CLA,it is most common to think of generating and propagating in the circumstances of binary addition, these concepts can be used more generally than this. The word digit can be replaced by bit when referring to binary addition of two. The addition of two 1-digit inputs A and B is set to generate if the addition always carry,irrespective of whether there is an input carry(less significant digits in the sum carry).for example in the decimal addition 52+67 of the tens digits 5 and 6 generates because the output carries to the hundred's digit irrespective of whether the ones digits carries referring the example,the ones digit do not have carry 2+7 ==9.

In the case of binary addition,a+b propagates if and only if both A and B are 1.if we write G(a,b) to represent the binary predicate that is true if and only if A.B Generates,we have:G(a,b)=a.b.The addition of two 1 –digit inputs a and N is said to propagate if the addition carry whenever there is an input carry. For example, in the decimal addition 37+62,the addition of the digits 3 and 6 propagates because the result would carry t the hundred's digit if the ones were to carry. Observe that propagation and generation are described with respect to the only one digit of addition and do not depend on any other digits in the sum.in the case of binary addition,a+b propagates if and only if atleast one of a or b is 1.if we write P(a,b) to represent the binary predicate that is true if and only if a+b propagates, we have

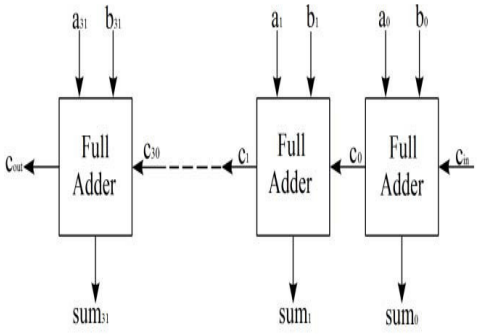
P (a,b)=a+b

Sometimes a different definition of propagation is used. By this definition a+b is said to be propagated if the addition carries whenever there is input carry,but will not carry if there is no input carry. Fortunately,Due to the way generate and propagate bits are used by the carry look ahead logic, it does not matter which definition is used. In the case of binary addition,this definition is expressed by : P(A,B)`=A xor B for binary arithmetic OR is faster than exclusive OR and takes few transistors to implement.However for a multiple- level CLA,it is simple to use P`(a,b) .gives these carries generates and propagates, a digit of addition carries precisely when either the addition generates or the next less significant bit(LSB) carries and the addition propagates. Written in Boolean algebra, with $C_i$the carry bit of digit i, and P_i and G_i the propagate and generate bits of digit i respectively.$C_{i+1}=G_i+(P_i.C_i)$[5].where G is carry generator.P is propagation carry. This can be elucidated in the operation of

the Ripple carry adder and carry look ahead adder.

Operation:

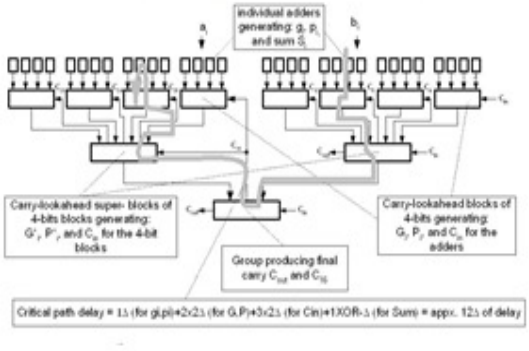
The operation of a 32 bit ripple carry adder can be explained by the circuitry of 32 bit RCA. The 32 bit RCA consists of 32 full adders which give carry and sum for each applied inputs. The inputs for the first full adder are assumed to be a_0, b0 and C_{in} these are the inputs where C_{in} is the input carryfor the first full adder. From this adder the sum is produced at the output. The circuit diagram of the 32 bit ripple carry adder is shown in fig.[1].The figure below gives us the details about the RCA where 32 full adders were used. The inputs are from a_0,b_0 to a_{31}, b31.The outputs are from S_0 to S_{31}.The full adder works based on the time delay.For example,if the first full adder gives output at 10 minutes (9:10) delay then the second adder gives the output with a delay of 10 more minutes (9:20).This delay continues till the last full adder.Finally the sum S_{31} andcarry C31 is obtained at last adder.This is how the 32 bit RCA works. Every full adder takes 10 minutes time to give the right output. We give carry input C_{in} as 0.If no carry is obtained at the first stage then operation of second adder will be impossible. In RCA the operation of second stage depends on the previous stage carry. The overall time to get the carry at the last adder C_{31} is 64 minutes. The time taken to get sum S_{31} is 63 minutes. Similarly for n bit RCA delay time for C_{out} is 2n minutes and for S_{out} is 2n-1.For many full adders in a single ripple carry adder ,say there are billion in number then computation of carry output for many inputs is not certainly practical.



Carry look ahead adder

We have seen that the ripple carry adder provides more delay in producing the output.so to overcome this we go for another adder called Carry look ahead adder(CLA).In carry lookahead adder it produces two carries namely propagation carry(P_i) and generation carry(G_i).Through this we can overcome the dependency of carry like as RCA.These can be calculated as follows. $G_i=a_i.b_i$, $P_i=a_{i+}b_i$ .Here i=0,1,..31.The carry equation for C is $C_{i+1}=G_i+P_i.C_i$[5]. For example to calculate similarly thenThe following figure shows the circuit of 32 bit carry look ahead adder. It consists of full adders which produce sum and carry. Here the operation is totally independent unlike the Ripple carry adder. This circuit mainly designed to reduce the propagation delay in generating the output. The carry look ahead adder is faster in execution. A carry look ahead adder is usually complex in structure than ripple carry adder.The following figure of a carry

look ahead adder elucidates the complexity of the adder where number of adders are used.



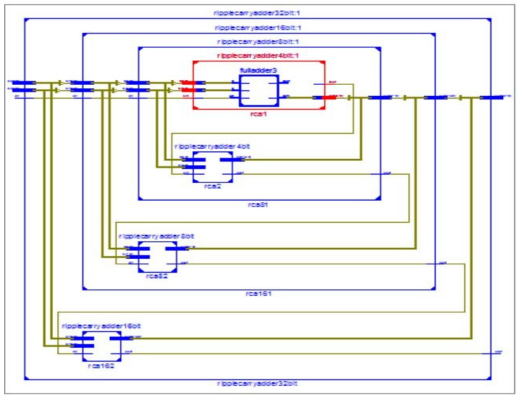
On adding more hardware,we can reduce the number of levels in the circuit and can fasten the things.we can cascade carry look ahead adders like ripple carry adders.This is more faster than RCA,for example for a 4-bit adder ,not much :CLA 4 gates,RCA 9 gates.but we cascade in a proper manner,for a 16 bit CLA 8 gates vs.33 gates. The delay of CLA grows logarithmically with the adder's size.Whilethe delay of RCA grows linearly.

Simulation:

we can analyse and implement the design of any circuit by hardware description language.in this paper we have implemented it using VHDL.The following simulation results shows the schematics of RCA and CLA.The Carry look a head adder is also called as Fast adder as it generates output With less Delay and high Speed.

Fig: simulated results of 32-bit RCA[1]

Fig:RTL schematic of 32-bit RCA[1]



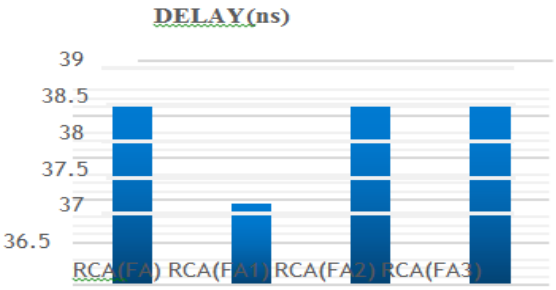


Fig:delay time in RCA.[1]

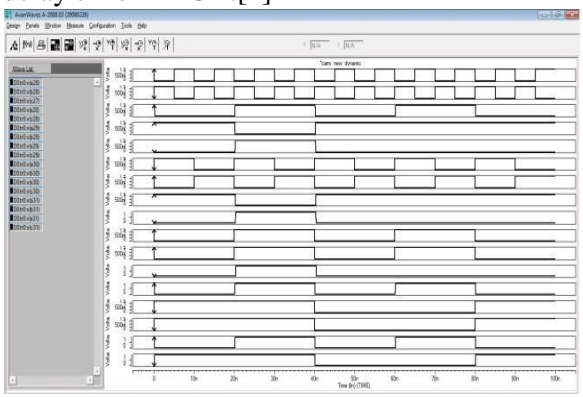


Fig:simulated results of CLA

These are the simulation results for 32 bit ripple carry adder and 32 bit carry look ahead adder.These are simulated in Xilinx 14.7 ISE suite design of Spartan 3e family

with delay -5.The codes for the adders can be written either in VHDL or Verilog HDL.By observing the sysnthesis report and simulation results we can compare the RCA with CLA.Through this we analysed that the delay in carry look ahead adder is less than that of ripple carry adder.

Comparison of RCA with CLA :

The comparison Table gives us the information about delay in ripple carry adder and carry look a head adder.The delay is more in case of ripple carry adder .While it is less in case of carry look ahead adder.The transistor count is also more in Carry look ahead adder ,Which makes it more complex in structure to design and implement.This is considered to be one of the major disadvantage of Carry look ahead adder.

Table 1 :comparison of delays in RCA and CLA

parameter	RCA (delay)	CLA (delay)
n bit	2n	5 or 3+2[lg n]
8 bit	16	5 or 8
32 bit	64	5 or 13
64 bit	128	5 or 15
Transistor count	1280	1514

Conclusion

From the above analysis it is evident that the delay time of 32-bit carry look ahead adder is less than that of 32-bit ripple carry adder.Trade –off between complexity and performance .ripple carry adders are simpler but slower. Carry look ahead adders are faster but more complex. Like ripple carry adder we need not to wait for the propagation of carries to get the sum. The disadvantage of CLA is that the carry logic block gets very complicated for more than four bits. For that reason CLA's are usually implemented as four bit modules and are used in hierarchical structure the realised adders that has multiples of four bits.

This analysis can further be extended to designing of 64-bit and 128 –bit.This can be simulated by using either Verilog or VHDL. Carry look ahead adder looks much better until we calculate the cost.

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