A REVIEW PAPER ON OPTIMIZATION OF PLACEMENT AND ROUTING TECHNIQUES

SHAIK KARIMULLAH [1] Dr. D.VISHNUVARDHAN[2]

1 Research Schlor at JNTUA Ananthapuramu. Email: Munnu483@gmail.com

2.Assistant Professor Department of ECE JNTUA Ananthapuramu Email: Vishnu.ece@jntua.ac.in

ABSTRACT:

Optimization techniques are one way to obtain operation and that will to extent possible, approach goals that have been set response to a given problem. As a result solutions such as designs for minimal operating cost, operating product quality, smallest device size and the like can be realized, Placement Routing is an important part of design step which determines physical arrangement of the logic blocks and connections among them the design. The quality of placement of logic blocks and connections among them determines overall performance of the logic implemented in the design. A few placement and routing optimization techniques like simulated annealing, quadratic, min-cut, and a hybrid approach of using genetic algorithm are reviewed in this paper. The method of evaluating each optimization technique along with its merits and demerits is provided in this paper. The Hybrid approach of using Genetic algorithm is implemented using MATLAB and the results are provided using Wire length driven Placement.

1. INTRODUCTION:

In ASIC design process, there is a need to find out performance of the layout. The key objective of Floor planning is to minimize the area of the chip as well as the delay. This can be achieved by proper placing of the logic blocks. Therefore it is important to predict the interconnections and thereby interconnection delay before the completion of actual routing. Normally it is difficult to predict the interconnects without knowing the source and destination blocks. Here the Logic design and the Physical design is carried out simultaneously and these designs help in better handling on timing and they also reduce the redesign time. Floor planning is a very important in the Top Down Physical design. We don't have particular criteria for floor planning, hence predicting routability is tough and hence the quality of Floor Planning is very hard in evaluation.

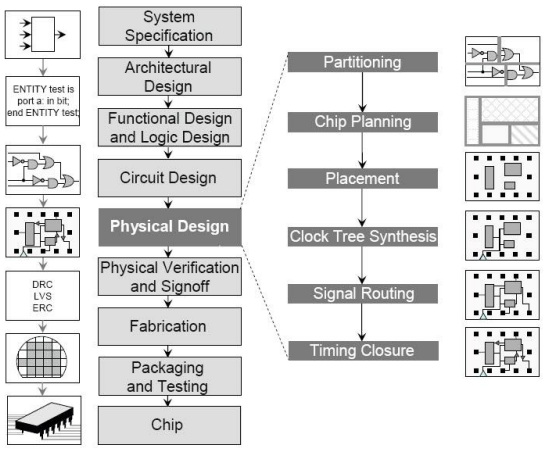

Fig. 1: ASIC design Flow

1.1 Placement Optimization objectives

Placement layout must be routable. In addition electrical effects like Cross talk or signal delay are to be considered. Due to lack of routing information the placer optimizes the estimates of routing quality metrics like Cut size , maximum signal delay, Wire congestion or Weighted Wire Length. For sustainable routing the main objective of Placement is Optimizing delays along the signal paths.

1.2 Routing Optimization goals

Routing Optimizing goals address to minimize total wire length and reduction of signal delays which are critical to overall chip timing in Gate array, Full Custom Design and Standard Cell design.

Placement and Routing are the primary requirements in Layout design. Based on Barkeley Building Block Layout System using complex placement and routing techniques, there is no guarantee of placement and routing solutions. In the recent past many new methods and verification techniques are developed to meet the market requirement. Some of these methods optimizes the ASIC verification in to two categories, Hardware based method and FPGA prototyping. Some other methods are listed below: Reusability method, Abstraction based method Assertion based method, Co-verification based method, Model based method etc.,

1.3 Overview of Existing Optimization Algorithms

Floor planning helps in determining the position/locations of the modules, in order to achieve minimum area and minimum wire- length. Different representation methods use different heuristic and meta-heuristic algorithms. Some examples of heuristic and meta-heuristic optimization algorithms are, Tabu search, Ant colony, Simulated Annealing and Genetic algorithm.

Simulated Annealing Algorithm

Simulated annealing algorithm was proposed by Kirkp atrick, 1980's; Gellat & Vecchi between 1982 – 1983 and by Cerny in 1985. The motivation for Simulated Annealing approach is to find the optimum solution based on the correlation among the hardening process of solids and solving large combinatorial optimization problem. Annealing process involves achieving a solid's bottom state by melting it at higher temperature, and slowly lowering the temperature (annealing), particles position themselves in the ground state [4].

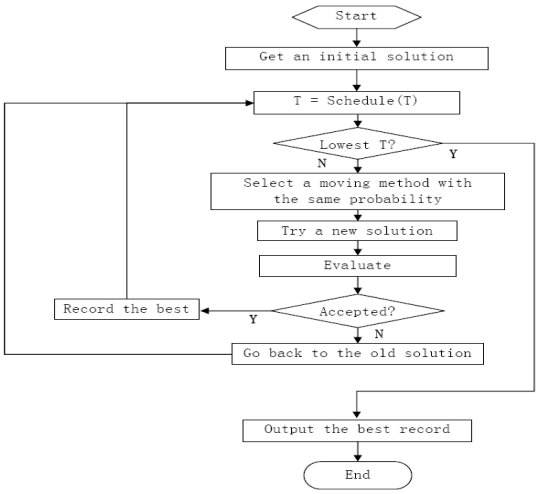

Fig. 2: Simulated Annealing

- First metal heating is done at a very high temperature.
- Crystal is formed as the temperature decreases.
- Higher energy state is obtained by decreasing the temperature very slowly.

The procedure of Simulated Annealing is given figure above.

Tabu Search Algorithm

Tabu search (TS) is one of the meta-heuristic approach for the problem of floor planning with non-slicing constraints. It comes into the category of iterative heuristics that are meant for providing solutions combinatorial optimization problems. It is a simplification of local search that hunts for the best change in the neighborhood of the current solution. Nevertheless, , TS does not get trapped in local optima like local search since it correspondingly agree to take bad moves if they are projected to lead unvisited solutions [3].

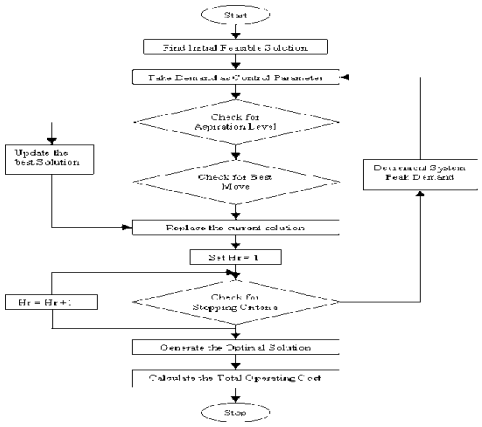

Fig.3 Tabu algorithm

Ant Colony Opitimization Algorithm

Ant Colony (AC) Optimization is a population based optimization that is used to find optimum solution for complex optimization problems. The Ant colony algorithm has three stages, initialization, construction and feedback. The initialization stage involves setting up the parameters like number of Ants and number of colonies. The construction phase involves the path construction based on pheromone concentration. The feedback stage includes the extraction and reinforcement of ants travelling experiences during path searching [5].

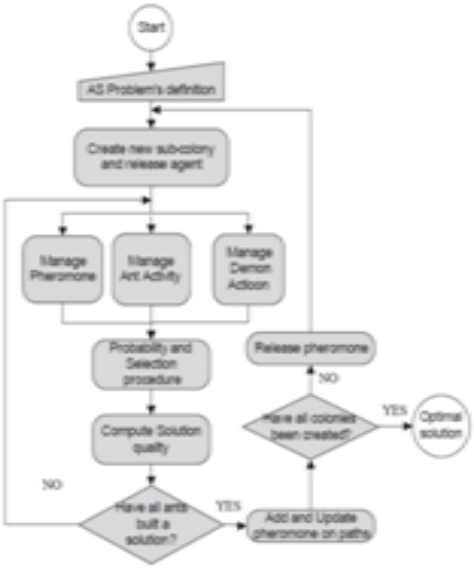

Fig. 4: Ant Colony Optimization Flow

The TSP also has a vital role in ACO search, finding the shortest distance in the middle of the Source and food. As seen in the flowchart given, initially the parameters are to be set. Select any city and construct path and ant moves to the selected city, if the distance achieved is small then stop the criteria otherwise update value and repeat the steps from setting parameters again.

Genetic Algorithm

The problem of achieving minimum area and minimum wire- length is solved using the Genetic algorithm. In this genetic algorithms. The working flow of Genetic algorithm is as shown below:

Genetic algorithm process flow:

- Consider the total population
- Select the best population of chromosomes
- Calculate the fitness function
- Mutation is applied to change the fitness value
- Cost calculation is done for every iteration
- If cost is minimum, then current

populationis treated as optimized result.

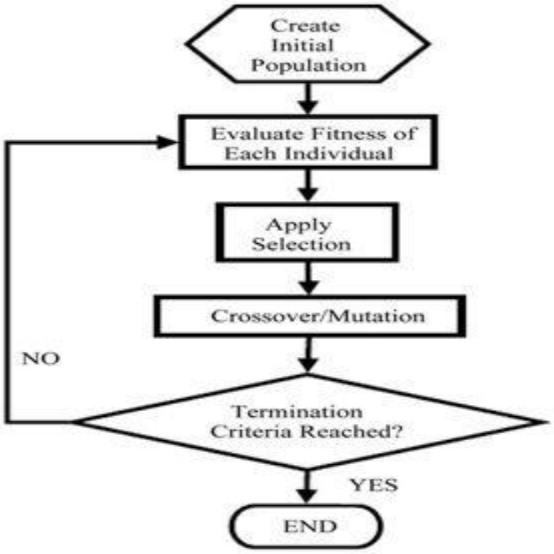

Fig. 5: Genetic Algorithm Flow Chart

Otherwise, this procedure continues until it gives a desired result.

The Placement Problem

The three common optimization criteria used for placement are Routability driven placement, Wrie length driven placement , Time length driven placemt..

Placement Optimization Techniques

Among the five available classes of FPGA placement optimization techniques, the hybrid method of Genetic algorithm and Simulated Annealing is better compared to Quadratic Simulated Annealing, Mincut, Particle Swarm Optimization
local minimum.

Optimization by Quadratic Placement

The following is the quadratic placement optimization technique proposed [4].

- Build and solve linear equations.
- Map the circuit to the FPGA chip.
- Add dummy nodes and expand the placement.
- Refinement for minimizing linear wire length.
- Repeat until there is not significant improvement.
- Refinement for minimizing linear wire length based on legal placement until there is no significant improvement.
- Re-map the circuit to the FPGAchip.

ROUTING TECHNIQUES:

Packet switched routers are used by onchip networks where the router can use buffering to buffer Flits when more number of Flits need the same output port. The routing can be done using Buffered routing and Bufferless Routing.

immediately to an output port. Since there

2. LITERATURE SURVEY

In 2016, k Sivasubramanianet al. [6] proposed a technique that concentrates on the reduction of area as an improvised harmony search algorithm and Twin memory Harmony search algorithm for VLSI floor planning. These two memories are initializes with HMS randomly generated. The results presented by this paper showed that the proposed algorithm THMS reduces different parameters like area, wire length, time.

In 2015, B.Premalatha et al. [7] proposed a new method for minimizing the wire length in FPGA Placement. In this, an different version of Particle Swarm Optimization algorithm called (ARPSO) “Attractive and Repulsive Particle Swarm Optimization Algorithm”. In ARPSO algorithm, the updating of velocity values is carried out depending on Diversity

factor D. The simulation results shows that proposed ARPSO algorithm is capable of optimized placement in FPGAs with minimal wire length.

In 2015, G Karimi et al. [8] introduced a technique for the placement of different sized modules in VLSI circuit design using "Multi Objective Particle Swarm Optimization, the author concentrated on reduction of cost function and wire length. The proposed algorithm was executed with the help of MATLAB and applied it for n100, n200 and n300 to GSRC benchmarks and achieved better run times and reduced overlap occurrence as well as wire length.

In 2015, D Gracia Nirmala Rani et al. [9] presented a novel differential evolution based optimization algorithm for non-slicable floor planning in VLSI. The floorplan structure is constructed using B*tree representation by taking feasible alignment constraint into consideration. The experiment results are placed as a table of comparison of algorithms SA, ESA, HAS, HGA and DE by taking area as parameter. All the algorithms are implemented on MCNC benchmark circuits and has generated promising results in placement.

In 2014, Shanavas et al. [10] proposed an algorithm for finding optimum solution for VLSI physical design Automation. The authors used Hybrid Genetic algorithm for finding solution. In this article the authors compiled entire physical design computations individually. Genetic Algorithm is used for global optimization. Simulated Annealing for local optimization. The results are formulated as tables with comparison of partitioning optimization using GA with Hybrid algorithms and floor planning optimization using GA with Hybrid algorithms. Placement optimization of Simulated Annealing compared with hybrid algorithms. Routing optimization of Simulated Annealing compared with hybrid algorithms.

In 2013, Xi Chen et al. [11] presented a concept regularity constrained floor planning where they have used Half Perimeter Wire Length (HPWL) model for estimation of wire length and area. This paper discusses about Longest Common Subsequence (LCS) packing algorithm that treats pre packed array blocks as a big block. The floor planning algorithms were implemented in c++ and the results were produced on MCNC benchmark circuits.

In 2013, Deen Md Abdullah et al, [12] introduced clonal selection algorithm for VLSI Floor planning Design. The authors considered preliminaries as floor plan representation, normalized polish expression, floor plan cost, cost function, artificial immune system, clonal selection algorithm. The results are tabulated with standard MCNC and GSRC benchmark in circuits.

In 2013, D Gracia Nirmala Rani et al. [13] a study on B*tree based evolutionary algorithms for optimization in VLSI floor planning. In this paper different optimization algorithms were discussed for floor planning like Fast Simulated Annealing, Simulate annealing embedded in tabu search, evolutionary and simulated annealing, Hybrid genetic algorithm, differential evolutionary algorithm. All these algorithms are compared by implementing on MCNC benchmark circuits.

In 2013, P Sivaranjani et al. [14] presented method of analyzing the performance of Floor planning in VLSI with the help of evolutionary algorithms. The paper discusses about different optimization algorithms like Particle Swarm Optimization, Hybrid Particle Swarm Optimization, Genetic Algorithm to achieve better placement results. The performance of algorithms is carried out on standard MCNC benchmark circuits by implementing the programs in MATLAB.

In 2012, T. Singha et al. [15] presented an

approach based on genetic algorithm for solving VLSI non-slicing floor planning problems. B* Tree structure is used to represent non slicing floor planning. Authors mentioned this approach of new genetic algorithm as Iterative Prototypes Optimization with Evolved Improvement (POEMS) algorithm. In this algorithm, Genetic algorithm is used to perform local search and it mainly focused on optimization of execution time of algorithm.

In 2011, P Hoyingcharoen et al. [16] proposed fault tolerance in sensor placement optimization using genetic algorithm. The paper aims to give minimum detection probability guaranteed. The authors have pointed the scenarios where sensor nodes fail as evaluator for fault tolerance as well as to use smallest number of sensor nodes to attain minimum detection probability even when some sensor nodes fails to function.

In 2011, Yiqiang Sheng et al. [17] proposed relay race algorithm with which the module placement in VLSI with minimum area to be achieved. The paper also presents comparison of Genetic algorithm, simulated annealing algorithm and the proposed relay race algorithm by which the worst cases of multi objective placement is shown. The experiments were conducted on standard MCNC ami49 benchmark circuit in which 50%improved performance in run time is observed.

In 2010 Jianli Chen et al, [18] shown comparative results of Hybrid genetic algorithm, mDA, Genetic algorithm and memetic algorithm for non slicing hard module VLSI floor planning with B*Tree representation. The results were shown based on MCNC benchmark circuits performance with HGA. In the results, it has shown that the area of circuit is reduced using Hybrid genetic algorithm.

3. CONCLUSION AND FUTURE WORK

In this paper, we have carried out a study on physical design floor planning problem in VLSI. The idea behind this study is to achieve minimum area and wire length while placing the modules in the chip design under floor planning process. The experimental investigation is carried out for 20 blocks with 50 iterations; Genetic algorithm has shown the promising results when compared to the other methods (Simulated annealing, Tabu search, Ant Colony) which were discussed in this paper. Hence these results motivate the researchers to do modifications in the available Genetic algorithm to achieve the results for multiple units.

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Author Profile:

Shaik Karimullah received his B.Tech Degree in ECE from MeRITS and M.Tech Degree in VLSI System Design from Madina Engineering College. Currently he is a research scholar at JNTUA Ananthapuramu.

Dr D.VishnuVardhan received his B.Tech Degree in ECE from RGM College of Engineering, Nandyal and M.Tech from JNTU Kakinada. Currently he is working as an Assistant Professor in the Department of ECE at JNTUA Ananthapuramu. His research interest includes Embedded Systems, Image Processing and VLSI System Design.