

Comparison of neural signals for ADC in Neural Implants

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Abstract: Low noise amplifiers used to benefit the patients suffering from paralysis by analysing the neural implants. The power consumption of the ADC directly depends on the architecture and construction of latched comparator. So it is advantageous to design the low noise latched comparator. In this work, the enhanced architecture for a latched comparator is implemented which is much useful in analysing neural implants. The proposed circuit will have less power dissipation than that of the existing architecture of latched comparators. In this paper, the proposed circuit is simulated using tanner EDA tools.

Keywords: ADC, latched comparator

1. INTRODUCTION:

In electronics, operational amplifier is designed to be used with negative feedback. It can be also used as comparator in loop configuration. Comparator is especially designed for open-loop configuration without any feedback. Hence it is the second most widely used device in electronic circuits after operational amplifier.

Comparators are mostly used in analog-to-digital converter(ADCs). In the conversion process, first the input signal is sampled. Then the sampled signal is applied to a number of comparators to determine the digital equivalent of the analog value. These are also used in peak detectors, Zero crossing detectors and switching power regulators.

Comparator is the device that compares two analog voltages or currents and switches its output to indicate which one is larger.

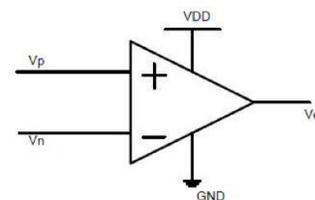


Fig 1: Schematic of Comparator

The above figure shows the Schematic diagram of comparator.

- If V_p is at greater potential than V_n , then the output V_o of the comparator is logic 1 and when V_p is at a potential less than V_n , the output is at logic 0.
- If we apply a pulse voltage at V_p and a DC reference voltage at V_n , the output is logic 1.
- When the pulse amplitude is greater than the reference voltage. The figure is shown below.

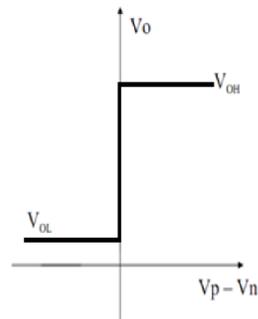


Fig 2: Voltage transfer characteristics of Ideal comparator.

The above figure shows the voltage transfer characteristics of Ideal comparator.

Thus a comparator compares two input analog values and gives binary output. In Ideal case, binary signals can have two values at any point. But actually there is a transition region between the two binary states. For a comparator, it is important to pass quickly through that transition region. Basically, comparators can be divided into two types.

First is the open loop comparators, which are nothing but operational amplifiers.

The second type is regenerative comparators. These comparators use positive feedback for the comparison of magnitude between two signals.

Types of Comparators:

There are two types of comparators

1. Static comparator
2. Dynamic comparator

Static Comparators:

- Static comparator needs a DC current for its operation, but can be used as a continuous time comparator i.e. no need of a strobe signal. These are open loop without feedback. The comparison is always active.
- The input of the comparator is always fixed.

Dynamic Comparators:

- Dynamic comparator doesn't need a DC current, but this needs a strobe signal to latch input.
- These always rely on positive feedback to speed up the decision. This feedback is implemented as a latch.
- These comparators changes with respect to output. These changes are generally done so to improve their noise immunity.

Characteristics of Comparator:

The Characteristics of comparator are,

- A. Static Characteristics
 - B. Dynamic Characteristics
- A) Static Characteristics:**

The Static characteristics of a comparator are

1. Gain
2. Offset Voltage
3. Input resolution
4. Noise
5. Input Common mode range

1. Gain:

Gain of a comparator can be expressed as,

$$\text{Gain (A}_v\text{)} = \text{Limit } V_{OH} - V_{OL} / \Delta V$$

Where ΔV = input voltage range

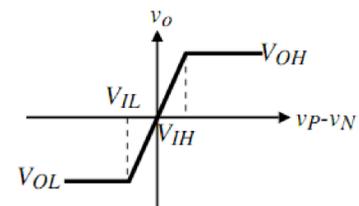


Fig 3: First order model of comparator

V_{IH} = Smallest input voltage for which the output voltage is V_{OH}

V_{IL} = Largest input voltage for which the output voltage is V_{OL}

2. Offset Voltage:

- The offset voltage is a parameter defining the differential DC voltage required between the inputs of an amplifier.
- Offset in the comparators are generated due to input transistor mismatches.

Input Offset Voltage:

The input offset voltage is the voltage which must be applied between the two input terminals to balance the amplifier.

Output Offset Voltage:

The Output Offset Voltage is defined as the DC voltage present at the output terminal of the comparator when the two input terminals are grounded.

3. Input Resolution:

It is the input voltage which is sufficient to make output swing to valid binary states.

4. Noise:

- Noise of a comparator is modeled if the comparator were biased in the transition region.
- This leads to an uncertainty in the transition region which causes Jitter.

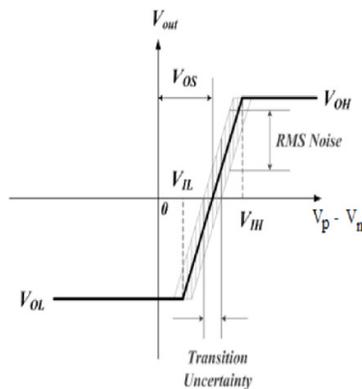


Fig 4: First order model of a comparator with input voltage and noise

5. Input Common mode Range (ICMR):

ICMR can be defined as the range of input voltage for which the comparator functions normally and meets all required specifications.

B) Dynamic Characteristics:

The dynamic characteristics are,

1. Propagation Delay
2. Slew rate
3. Speed

1. Propagation Delay:

Propagation Delay is defined as at how much speed the amplifier responds with applied input. i.e. the delay between output and input.

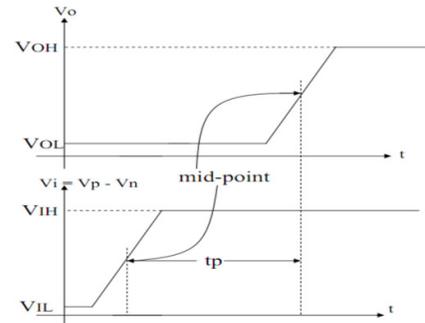


Fig 5: Propagation delay of a comparator

Propagation Time Delay = (Rising Propagation delay time + Fall Propagation delay time)/2.

2. Slew Rate:

- The Slew rate of an Operational Amplifier or an amplifier circuit is the rate of change in the output voltage caused by a step change on the input.
- It is measured as a voltage change in a given time, typically V/usec or V/msec.

3. Speed:

Speed is the inverse of propagation delay.

$$\text{Speed} = 1 / \text{Propagation Delay}$$

Problems in Comparators:

The problems faced in comparators are

1. Thermal Noise
2. Kick back Noise

1. Thermal Noise:

Thermal noise is also called as Johnson noise. It is the electronic noise generated by the thermal agitation of the charge carriers inside an electrical conductor at equilibrium, which happens regardless of any applied voltage. The power spectral density of thermal noise is nearly constant throughout the frequency spectrum.

2.Kick back Noise:

The large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of comparator. Since the circuit preceding it doesn't have zero output impedance, the input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called Kick back noise.

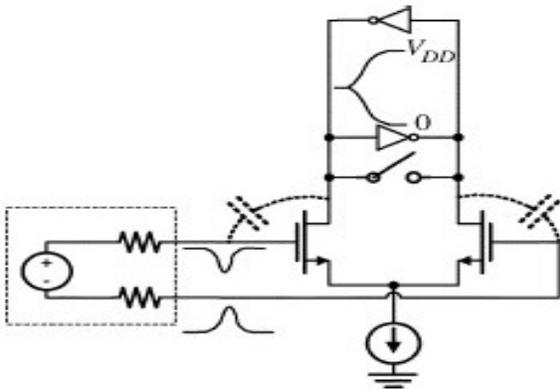


Fig 6: Kick back noise Generation.

Operation:

In reset mode, when the switch is close to the transistor, current depends on the input voltage. There will be small output voltage because the switch has non-zero resistance. In the comparison mode when the switch is open, the two cross coupled inverters implement a positive feedback, this makes the output voltage go towards 0 and VDD. By using latched comparators we can reduce the Kick back noise.

2.Existing Architectures of Latched Comparator:

Due to strong positive feedback in the regenerative latch clocked regenerative comparators have found wide applications In many high speed ADCs since they can make fast decisions.single tail comparator and conventional double tail dynamic comparator are the existing comparators.

Single Tail Comparator:

Single tail comparators have higher input impedance. Due to the presence of high input resistance, the power consumed is low which results in less static power consumption. The tail transistor increases the speed of the circuit when compared to the pre amplifier circuit as fast switching of PMOS and NMOS occurs. The circuit diagram of single tail comparator is shown in figure.

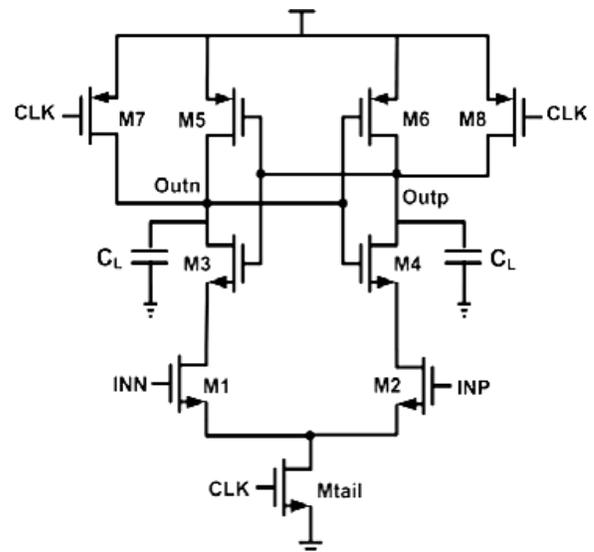


Fig 7: Single Tail Comparator.

Operation :

There are two phases in the operation of single tail comparator. They are
 1.RESET phase
 2.Comparison phase

1.RESET phase:

When clk=0 the circuit operates in reset phase. In this phase tail transistor gets off and transistors M7 and M8 pul both outputs outp and outn to VDD. This is the start condition of the circuit.

2.COMPARISON phase:

When CLK=VDD, this circuit operates in comparison mode. In this phase Mtail transistor is ON and M7,M8 transistors become OFF state. Both the outputs of the transistors outn and outp which have been precharged to VDD starts to discharge

with different discharging rates depending the input voltage applied.

- When $V_{INP} > V_{INN}$, outp discharges faster than outn. i.e, when outp falls to VDD before outn the transistor M5 will turn ON on initiating the latch generation caused by inverters in back to back connections(M3,M5,M4,M6).Thus, outn discharges to VDD and outp discharges to GND.
- If $V_{INP} < V_{INN}$, the circuit works vice versa.

But the single tail comparator have only one path for the flow of current in the circuit. AS more number of transistors are placed in above have of the circuit as shown above, it experiences stacking and due to this high supply voltage is required for the operation. To overcome these limitations, we go for another circuit by adding another tail transistor called as double tail comparator.

Double Tail Comparator:

The circuit is built with 5 PMOS transistors and 7 NMOS transistors. The circuit diagram of double tail comparator is shown below.

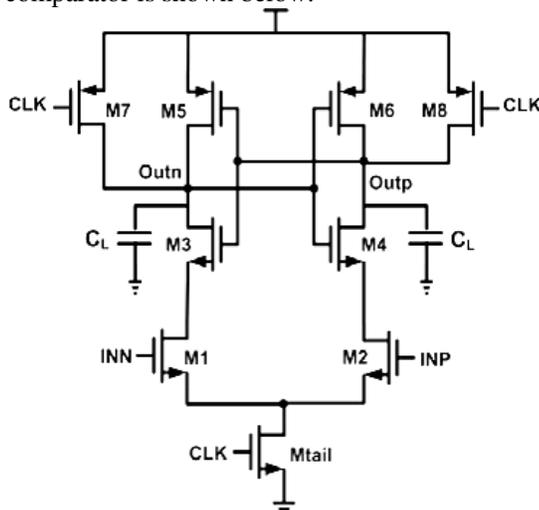


Fig 8: Double Tail Comparator.

Operation:

1. RESET PHASE:

When $CLK=0$ the circuit operates in reset phase. In this phase Mtail1 and Mtail2 transistors are OFF, transistors M3 and M4 charge their nodes outp and outn to VDD.

2. COMPARISON PHASE:

In comparison phase, when $CLK=VDD$ Mtail1 and Mtail2 gets ON, transistors M3 and M4 turn OFF. The output voltages at nodes outp and outn start to drop with a rate defined by Mtail1.

3. Proposed Comparator Design:

The design of the 3-stage dynamic comparator is shown in the below figure.

Operation:

The proposed comparator comprises 3 stages. When the clock is high, the input transistors begin to discharge V_{x1} and V_{x2} nodes that drive the PMOS input pairs of the second stage. When these nodes become sufficiently low, the nodes V_{y1} and V_{y2} gets charged toward VDD. When these nodes are suitably charged, the third stage starts the regeneration phase. Due to positive feedback from the cross coupled inverters and pre-amplification gain from the first two stages, outputs regenerate quickly. Large pre amplification gain from the first two dynamic integration stages sufficiently reduces the regeneration time to help meeting the timing specification of the proposed architecture. Comparator offset is foreground calibrated by adjusting C_{lap} and C_{alm} . Since DAC redundancy is provided after $2b/cycle$ conversions and can tolerate as large as 10 mV offset mismatch among 3 comparators, the proposed ADC does not need precise comparator mismatch calibration. Only coarse calibration is enough to achieve the targeted performance specifications.

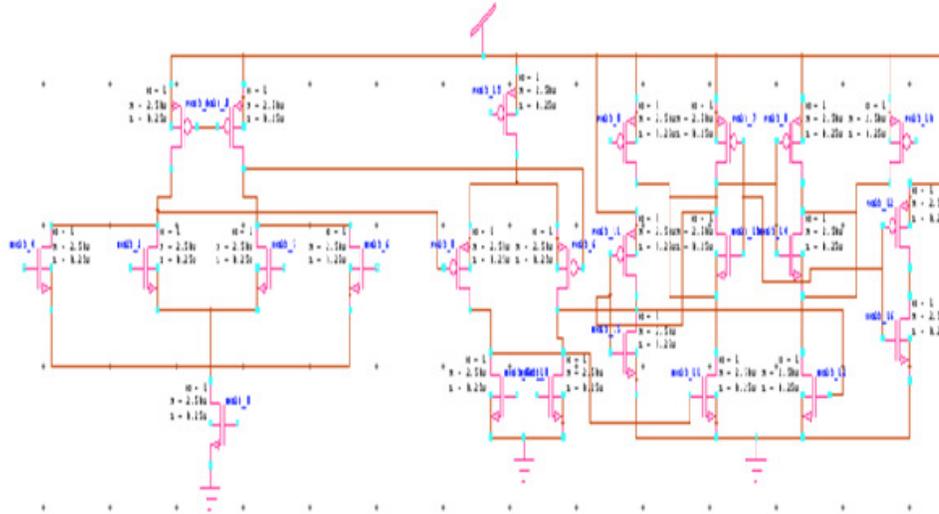


Fig 9: Proposed Comparator design

In this paper we design the latched comparator and simulate the circuit by using TANNER software. Firstly, we design the proposed circuit by using S EDIT. The input of the design is clock signal.

When CLK=0 all the PMOS transistors turn ON and NMOS transistors turn OFF. In this condition the PMOS transistors act as short circuit and the output is charged to VDD.

When CLK=1 or VDD then all NMOS transistors turns ON and PMOS transistors turns OFF. In this condition NMOS acts as short circuit and output is discharged to GND.

In this proposed architecture of latched comparator two conditions are existed. They are

If $V_{INP} > V_{INN}$, the output node outp discharges fastly to VDD than the output node outn.

- If $V_{INP} < V_{INN}$, the output node outn discharges fastly to GND than the output node outp.

4. Simulation Results

The Transient response of the proposed comparator is depicted in the fig 12.

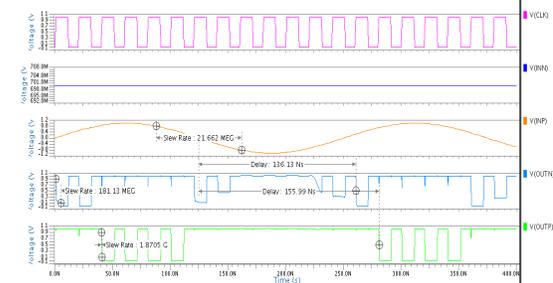


Fig 12: Transient analysis of proposed comparator

Here the comparison is done as explained in the operation of proposed comparator.

Table 1: Comparison table.

Type of comparator	Power dissipation	Kickback noise
Single tail	1.063 nW	1667.6 mv
Double tail	2.3 nW	1045.29 mv
Proposed comparator	1.902 nW	969.9 mv

From the comparison table it is evident that proposed comparator dissipates low power and also suffers from low kickback noise when compared with the other architectures.

5. Conclusion

REFERENCES

- [1] M. Malik, T. Cochrane, D. W. Davies, and A. J. Camm, "Clinically relevant computer model of cardiac rhythm and pacemaker/heart interaction," *Med. Biol. Eng. Comput.*, vol. 25, no. 5, pp. 504–512, 1987.
- [2] Gerrish, E. Herrmann, L. Tyler, and K. Walsh, "Challenges and constraints in designing implantable medical ICs," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 435–444, Sep. 2005.
- [3] S. Kim and M. Song, "An 8-bit 200MSPS CMOS A/D converter for analog interface module of TFT-LCD Driver," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2001, vol. 1, pp. 528–531.
- [4] S. Babayan-Mashhadi and R. Lotfi, "Analysis and design of a low-voltage low-power double-tail comparator," *IEEE Transactions on Very Large Scale Integr. (VLSI) Syst.*, [Online]. Available: <http://dx.doi.org/10.1109/TVLSI.2013.2241799>.
- [5] B. Razavi, *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, New York, 2001).
- [6] P. Nuzzo, F. De Bernardinis, P. Terreni, G. Van der Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," *IEEE Trans. Circuits Syst. I* 55(6), 1441–1454 (2008).
- [7] Ka-Meng Lei, Pui-In Mak, Rui P. Martins, "Systematic Analysis and Cancellation of Kickback Noise in a dynamic Comparator," *Analog Integrated Circuits and Signal Processing*, Vol. 77, pp. 277–284.
- [8] Pedro M. Figueiredo and Joao. C. Vital, "Kickback Noise Reduction Techniques for CMOS Latched Comparators," *IEEE Transactions on Circuits and Systems-II*, Vol. 53, No. 7, July 2006.
- [9] Howard Tang, Zhuo Chao Sun, Kin Wai Roy Chew and Lier Siek, "A 5.8 nW 9.1-ENOB 1-ks/s Local Asynchronous Successive Approximation Register ADC for Implantable Medical Devices", *IEEE Transactions on Very Large Scale*

Integration (VLSI) Systems.

[10] Zhangming Zhu, and Yuhua Liang, "A 0.6-V 38-nW 9.4-ENOB 20-ks/s SAR ADC in 0.18- μ m CMOS for Medical Implant Devices", *IEEE Journal of solid state circuits*, Vol. 62, NO-9, and September 2015.

[11] Dai Zhang, Ameya Bhide, Atila Alvandpour, "A 53-nW 9.1-ENOB 1-ks/s SAR ADC in 0.13- μ m CMOS for Medical Implant Devices", *IEEE Journal of solid state circuits*, Vol. 47, NO-7, and July 2012.

In this paper, the latched comparator for neural application is proposed and simulated with a supply of 1 v by using 130 nm CMOS Technology. The parameters like power dissipation and kickback noise are measured to analyze the performance of the proposed comparator. The proposed comparator consumes less power and also has low kickback noise as compared to the other architectures.

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