DESIGN OF ARITHMETIC AND LOGIC UNIT USING CARBON NANOTUBE FIELD EFFECT TRANSISTOR

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***Abstract*—CNTFET is the carbon nanotube field effect transistor that has better performance, high speed, less power consumption and temperature tolerance compared to CMOS design. To overcome drawbacks such as leakage current, short-channel effect and power consumption CNTFET is an one among attractive alternatives in nanotechnology.**

***Keywords*—** Carbon Nanotubes field-effect transistor (CNTFET), Logic gates.

I. INTRODUCTION

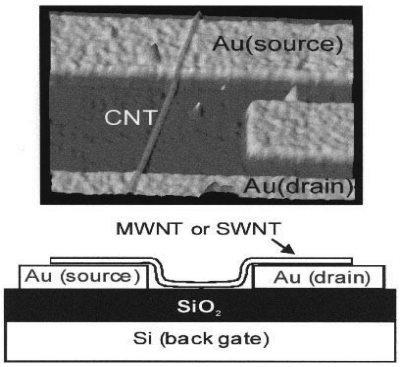
Over the past few years, critical dimensions of silicon transistor devices have decreased dramatically. Prototype transistors with gate length in 30-nm range have been successfully fabricated and were found to exhibit excellent electrical characteristics. While there is still some room for further improvements, the consensus is that alternative concepts will become necessary at some point in future. Since the early 1970s the conventional advancement in technology has followed Moore's law (Moore 1975) whereby the number of transistors incorporated on a memory chip doubles every year and a half. This has resulted from continual improvements in design factors such as interconnectivity efficiency as well as from continual decrease in size. The phenomenal progress signified by Moore's law has been achieved through scaling of the metal-oxide-semiconductor field effect transistor (MOSFET) from larger physical dimensions to smaller physical dimensions, thereby gaining speed and density. Shrinking the conventional MOSFET beyond the 50 nm-technology node requires innovations to circumvent barriers due to fundamental physics that constrains the conventional MOSFET. With the end of silicon transistors scaling, a great deal of research activity is currently focused on identifying alternatives which would enable continued improvements in the density and performance of electronics information systems. Other alternatives for more density and performance of electronics information systems are high dielectric constant (high- k) gate dielectric, metal gate electrode, double-gate FET, and strained-Si FET. High dielectric-constant materials are useful as gate insulators as they can provide efficient charge injection into transistor channels and reduce direct tunneling leakage currents. Of the various materials systems and structures being investigated carbon nanotubes have shown the promising characteristics. Carbon nanotubes are hollow seamless cylinders that can be envisioned as being formed by rolling up a finite sized piece of graphite sheet. Depending on how the roll-up of the graphite sheet occurs during the growth process, carbon nanotubes can exhibit semiconducting as well as metallic. Moreover, the band gap of the semiconducting tubes scales inversely with the tube diameter. The growth process can be tuned such that fine control of the tube diameter is achieved thereby forming semiconducting tubes with very similar electrical properties. Growth conditions giving the best yield produce carbon nanotubes with a diameter of around 1.4 nm.

In addition, the confinement helps to control in particular the transistor off-state when semiconducting carbon nanotubes are used in a field-effect transistor (CNTFET) geometry. Thus, carbon nanotube field effect transistors (CNTFETs) are particularly attractive due to the possibility of near ballistic channel transport, easy application of high-k gate insulator and novel device physics. The CNTFETs were simulated by solving the Schrödinger equation using the non-equilibrium Green's function (NEGF) formalism, self-consistently with the poisson equation. Ballistic transport was also assumed. In this paper, a review of vertically scaled carbon nanotubes field effect transistors is presented and it is shown that these devices exhibit excellent electrical characteristics, including steep sub-threshold slope and high transconductance.

II. FABRICATION AND PERFORMANCE OF CARBON NANOTUBE FETS

FETs, particularly in CMOS form, have been proven to be the most technologically useful device structures. It is, thus, natural that we have chosen to build such devices using CNTs. The first such devices were fabricated. In these a single SWCNT was used to bridge two noble metal electrodes prefabricated by lithography on an oxidized silicon wafer. The SWCNT

played the role of the "channel," while the two metal electrodes functioned as the "source" and "drain" electrodes.



CNTFETs. Bottom: Schematic cross section

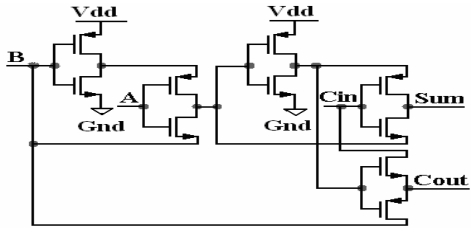
III. CARBON NANOTUBE INTEGRATED CIRCUITS:

LOGIC GATES:

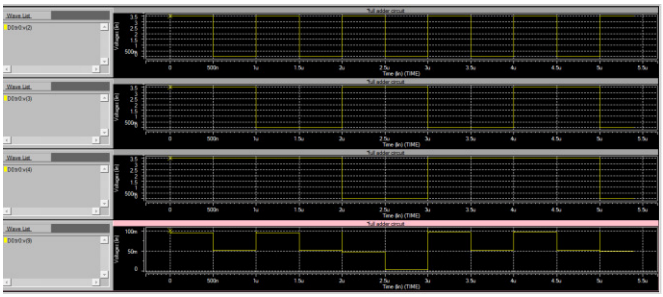
.In 2001 we demonstrated that this was possible by fabricating a CMOS-like voltage inverter (a logic NOT gate. For simplicity, we used the early design of CNTFETs involving the CNT on top of gold electrodes we show the structure and electrical characteristics of an inverter circuit involving a n- and a p-CNTFETs. Originally, both CNTFETs were p-type because of their exposure to air (oxygen). We then covered one of them by a protective film of PMMA (a more stable protection is provided by a SiO film while the other was left unprotected. Both of the CNTFETs were then annealed under vacuum, which transformed both of them into n-type. After cooling, the pair was exposed to oxygen, which converted the unprotected CNTFET to p-type, while the protected one remained n-type. In this way, the two complementary CNTFETs needed were formed and wired. The inverter works the same way as an ordinary CMOS inverter. The input voltage is applied simultaneously to the gates of the complementary CNTFET.

IV. PROPOSED SYSTEM

Full Adder is the core element of complex arithmetic circuits like addition, multiplication, division, exponentiation, and so forth. There are standard implementations with various logic styles that have been used in the past to design full-adder cells and the same are used for comparison in this paper. Although they all have similar function, the way of producing the intermediate nodes and the transistor count is varied. Different logic styles tend to favor one performance aspect at the expense of the others. The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. The circuit delay is determined by the number of inversion levels, the number of transistors in series, transistor sizes and intracell wiring capacitance Circuit size depends upon the number of transistors, their sizes and on the wiring complexity. Some of them use one logic style for the whole full adder while the other use more than one logic style for their implementation.



Full Adder Circuit

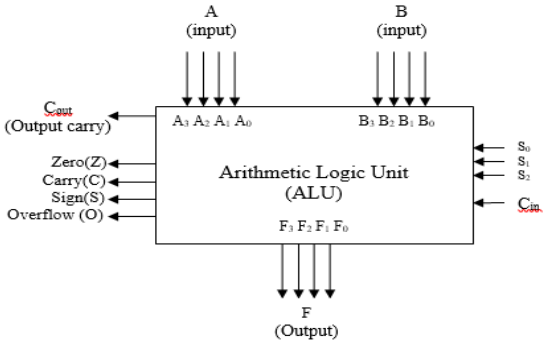


Simulation Output of Full Adder Circuit

V.DISCUSSION

Conventional Complementary metal oxide semiconductor circuits (CMOS) dissipate energy in the form of bits of

information. This dissipation of energy is in the form of power dissipation and plays a very important role as far as low power design is considered. Today, most digital circuits are being designed using Reversible Logic. Design based on Reversible Logic helps in reducing heat dissipation, allowing nearly energy free computation, allowing higher circuit densities and enabling better test of faults. In this paper, a novel design for a 8-bit ALU is proposed. The 8-bit ALU is designed by cascading 1- bit ALU. The two major units of a 1-bit ALU are the control unit and the adder unit. For the control unit, the control output gate has been used. The most significant aspect of this paper is that as compared to other papers, this ALU design has reduced gate count, and transistor count.



8-bit ALU Circuit

VI. Conclusion

Thus, we conclude that the simulation results demonstrate the superiority of the proposed structures in terms of speed, power consumption, and power-delay-product enhance the performance of proposed design.

VII. Referance

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