

Study on Topologies Multi Level Inverters

Bachwad M.R. , Maske Ashadeep M

Department of Electrical Engineering , Govt. College of Engg. Aurangabad

Abstract:

Multilevel inverters have become more popular over the years in electric high power application with the promise of less disturbances and the possibility to function at lower switching frequencies than ordinary two-level inverters. This paper presents information about several multilevel inverter topologies, such as the Neutral-Point Clamped Inverter and the Cascaded Multi cell Inverter. These multilevel inverters will also be compared with two-level inverters in simulations to investigate the advantages of using multilevel inverters. Modulation strategies, component comparison and solutions to the multilevel voltage source balancing problem will also be presented in this work.

Keywords — **multilevel, Neutral-clamped, PWM.**

I. INTRODUCTION

A device that converts DC power into AC power at desired output voltage and frequency is called an Inverter. Phase controlled converters when operated in the inverter mode are called line commutated inverters. But line commutated inverters require at the output terminals an existing AC supply which is used for their commutation. This means that line commutated inverters can't function as isolated AC voltage sources or as variable frequency generators with DC power at the input. Therefore, voltage level, frequency and waveform on the AC side of the line commutated inverters can't be changed. On the other hand, force commutated inverters provide an independent AC output voltage of adjustable voltage and adjustable frequency and have therefore much wider application.

Inverters can be broadly classified into two types based on their operation:

- Voltage Source Inverters(VSI)
- Current Source Inverters(CSI)

Voltage Source Inverters is one in which the DC source has small or negligible impedance. In other words VSI has stiff DC voltage source at its input terminals. A current source inverter is fed with adjustable current from a DC source of high impedance, i.e.; from a stiff DC current source. In a CSI fed with stiff current source, output current waves are not affected by the load.

From view point of connections of semiconductor devices, inverters are classified as under

- Bridge Inverters
- Series Inverters
- Parallel Inverters

II. DIFFERENT TOPOLOGIES OF MULTILEVEL INVERTERS

The basic three types of multilevel topologies used are:

1. Diode clamped multilevel inverters
2. Flying capacitors multilevel inverter or capacitor clamped multilevel inverter
3. Cascaded inverter with separate DC sources.

1. Diode Clamped Multilevel Inverter

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter [10]. A three-level diode clamped inverter consists of two pairs of switches and two diodes. Each switch pairs works in complimentary mode and the diodes used to provide access to mid-point voltage. In a three-level inverter each of the three phases of the inverter shares a common dc bus, which has been subdivided by two capacitors into three levels [8]. The DC bus voltage is split into three voltage levels by using two series connections of DC capacitors, C1 and C2. The voltage stress across each switching device is limited to Vdc through the clamping diodes Dc1 and Dc2. It is assumed that the total dc link voltage is Vdc and mid point is regulated at half of the dc link voltage, the voltage across each capacitor is $V_{dc}/2$ ($V_{c1}=V_{c2}=V_{dc}/2$).

In a three level diode clamped inverter, there are three different possible switching states which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate. For a three-level inverter, a set of two switches is on at any given time and in a five-level inverter, a set of four switches is on at any given time and so on. Figure 1 shows the circuit for a diode clamped inverter for a three-level and a five-level inverter.

Switching states of the three level inverter are summarized in table 1

Table 1 Switching States in One Leg of the Three-Level Diode Clamped Inverter

Switch Status	State	Pole Voltage
$S_1=ON, S_2=ON$ $S_1'=OFF, S_2'=OFF$	$S=+ve$	$V_{ao}=V_{dc}/2$
$S_1=OFF, S_2=ON$ $S_1'=ON, S_2'=OFF$	$S=0$	$V_{ao}=0$
$S_1=OFF, S_2=OFF$ $S_1'=ON, S_2'=ON$	$S=-ve$	$V_{ao}=-V_{dc}/2$

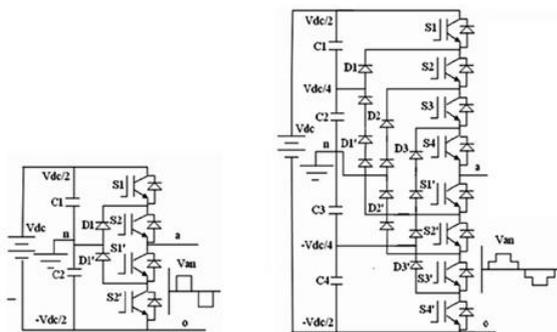


Figure 1 Topology of the Diode-Clamped Inverter (a) Three-Level Inverter, (b) Five-Level Inverter.

Figure 2 shows the phase voltage and line voltage of the three-level inverter in the balanced condition. The line voltage V_{ab} consists of a phase-leg a voltage and a phase-leg b voltage. The resulting line voltage is a 5-level staircase waveform for three-level inverter and 9-level staircase waveform for a five-level inverter. This means that an N-level diode-clamped inverter has an N-level output phase voltage and a $(2N-1)$ -level output line voltage. In general the voltage across each capacitor for an N level diode clamped inverter at steady state is $V_{dc}/(N-1)$. Although each active switching device is required to block only a voltage level of V_{dc} , the clamping diodes require different ratings for reverse voltage blocking [7].

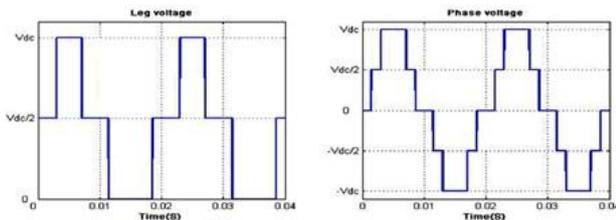


Figure 2 Output Voltage in Three Level Diode Clamped Inverter (a) Leg Voltage (b) Output Phase Voltage

In general for an N level diode clamped inverter, for each leg $2(N-1)$ switching devices, $(N-1) * (N-2)$ clamping diodes and $(N-1)$ dc link capacitors are

required. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform. However, capacitor voltage balancing will be the critical issue in high level inverters. When N is sufficiently high, the number of diodes and the number of switching devices will increase and make the system impracticable to implement. If the inverter runs under pulse width modulation (PWM), the diode reverse recovery of these clamping diodes becomes the major design challenge. The structure is more complicated than the two-level inverter; the operation is straight forward [11].

III.PULSE MODULATION SCHEMES

In PAM the successive sample values of the analog signal $s(t)$ are used to effect the amplitudes of a corresponding sequence of pulses of constant duration occurring at the sampling rate. No quantization of the samples normally occurs (Fig. 1a, b). In principle the pulses may occupy the entire time between samples, but in most practical systems the pulse duration, known as the duty cycle, is limited to a fraction of the sampling interval. Such a restriction creates the possibility of interleaving during one sample interval one or more pulses derived from other PAM systems in a process known as time-division multiplexing (TDM).

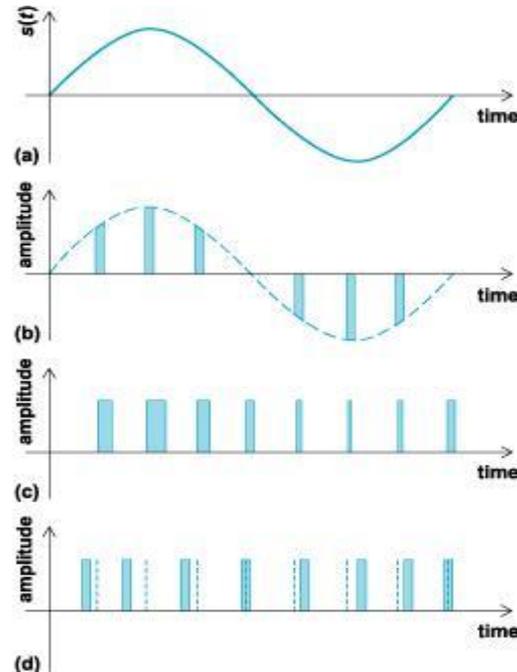


Figure 3(a) Analog signal, $s(t)$. (b) Pulse-amplitude modulation. (c) Pulse-width modulation. (d) Pulse position modulation

• Pulse-width modulation

In PWM the pulses representing successive sample values of $s(t)$ have constant amplitudes but vary in time duration in direct proportion to the sample value. The pulse duration can be changed relative to fixed leading or trailing time edges or a fixed pulse center. To allow for

time-division multiplexing, the maximum pulse duration may be limited to a fraction of the time between samples.

- Pulse-position modulation

PPM encodes the sample values of $s(t)$ by varying the position of a pulse of constant duration relative to its nominal time of occurrence. As in PAM and PWM, the duration of the pulses is typically a fraction of the sampling interval. In addition, the maximum time excursion of the pulses may be limited (Fig. 1d).

- Pulse-code modulation

Many modern communication systems are designed to transmit and receive only pulses of two distinct amplitudes. In these so-called binary digital systems, the analog-to-digital conversion process is extended by the additional step of coding, in which the amplitude of each pulse representing a quantized sample of $s(t)$ is converted into a unique sequence of one or more pulses with just two possible amplitudes. The complete conversion process is known as pulse-code modulation. Figure 2a shows the example of three successive quantized samples of an analog signal $s(t)$, in which sampling occurs every T seconds and the pulse representing the sample is limited to $T/2$ seconds. Assuming that the number of quantization levels is limited to 8, each level can be represented by a unique sequence of three two-valued pulses

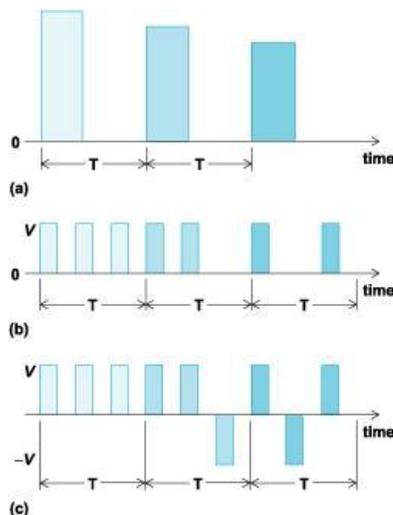


Figure 4(a) Three successive quantized samples of an analog signal. (b) With pulses of amplitude V or 0 . (c) With pulses of amplitude V or $-V$

PCM enjoys many important advantages over other forms of pulse modulation due to the fact that information is represented by a two-state variable. First, the design parameters of a PCM transmission system depend critically on the bandwidth of the original signal $s(t)$ and the degree of fidelity required at the point of reconstruction, but are otherwise largely independent of the information content of $s(t)$. This fact creates the possibility of deploying generic transmission systems suitable for many types of information. Second, the detection of the state of a two-state variable in a noisy environment is inherently simpler than the precise

measurement of the amplitude, duration, or position of a pulse in which these quantities are not constrained. Third, the binary pulses propagating along a medium can be intercepted and decoded at a point where the accumulated distortion and attenuation are sufficiently low to assure high detection accuracy. New pulses can then be generated and transmitted to the next such decoding point. This so-called process of repeating significantly reduces the propagation of distortion and leads to a quality of transmission that is largely independent of distance.

Why pulse width modulation?

Pulse-width modulation (PWM) of a signal or power source involves the modulation of its duty cycle, to either convey information over a communications channel or control the amount of power sent to a load.

Advantages of PWM

Using pulse width modulation has several advantages over analog control.

1. The entire control circuit can be digital, eliminating the need for digital-to-analog converters.
2. Using digital control lines will reduce the susceptibility of your circuit to interference.
3. Finally, motors may be able to operate at lower speeds if you control them with PWM. When you use an analog current to control a motor, it will not produce significant torque at low speeds.
3. The output voltage control can be obtained without any additional components.
4. With this method, lower order harmonics can be eliminated or minimized Along with its output voltage control.
5. As higher order harmonics can be filtered easily the higher order harmonics can be minimized.

IV. APPLICATIONS

- Dc power source utilization

Inverter designed to provide 115 VAC from the 12 VDC source provided in an automobile. The unit provides up to 1.2 Amps of alternating current, or just enough to power two sixty watt light bulbs.

An inverter converts the DC electricity from sources such as batteries, solar panels, or fuel cells to AC electricity. The electricity can be at any required voltage; in particular it can operate AC equipment designed for mains operation, or rectified to produce DC at any desired voltage.

Grid tie inverters can feed energy back into the distribution network because they produce alternating current with the same wave shape and frequency as supplied by the distribution system. They can also switch

off automatically in the event of a blackout.

Micro-inverters convert direct current from individual solar panels into alternating current for the electric grid.

- Uninterruptible power supplies

An uninterruptible power supply is a device which supplies the stored electrical power to the load in case of raw power cut-off or blackout. One type of UPS uses batteries to store power and an inverter to supply AC power from the batteries when main power is not available. When main power is restored, a rectifier is used to supply DC power to recharge the batteries.

It is widely used at domestic and commercial level in countries facing Power outages.

- Induction heating

Inverters convert low frequency main AC power to a higher frequency for use in induction heating. To do this, AC power is first rectified to provide DC power. The inverter then changes the DC power to high frequency AC power.

- HVDC power transmission

With HVDC power transmission, AC power is rectified and high voltage DC power is transmitted to another location. At the receiving location, an inverter in a static inverter plant converts the power back to AC.

- Variable-frequency drives

A variable-frequency drive controls the operating speed of an AC motor by controlling the frequency and voltage of the power supplied to the motor. An inverter provides the controlled power. In most cases, the variable-frequency drive includes a rectifier so that DC power for the inverter can be provided from main AC power. Since an inverter is the key component, variable-frequency drives are sometimes called inverter drives or just inverters.

- Electric vehicle drives

Adjustable speed motor control inverters are currently used to power the traction motor in some electric locomotives and diesel-electric locomotives as well as some battery electric vehicles and hybrid electric highway vehicles such as the Toyota Prius. Various improvements in inverter technology are being developed specifically for electric vehicle applications.^[2] In vehicles with regenerative braking, the inverter also takes power from the motor (now acting as a generator) and stores it in the batteries.

- The general case

A transformer allows AC power to be converted to any desired voltage, but at the same frequency. Inverters, plus rectifiers for DC, can be designed to convert from any voltage, AC or DC, to any other voltage, also AC or DC, at any desired frequency. The output power can never exceed the input power, but efficiencies can be high, with a small proportion of the power dissipated as waste heat.

V. CONCLUSION

This paper provides a comprehensive study on multilevel inverter topologies. Every topology has been described in detail.

Today, more and more commercial products are based on the multilevel inverter structure, and more and more worldwide research and development of multilevel inverter-related technologies is occurring.

REFERENCES

- [1] P.S. Bhimbra, Power Electronics.
- [2] M Rashid, Power Electronics.
- [3] Muhammad Ali Mazidi and Janice Gillispie Mazidi, "The 8051 Microcontroller and Embedded Systems, Pearson Prentice Hall Publication".
- [4] L Li, D Crazkowski, P Pillay, Y. Liu "Multilevel Selective Harmonic Elimination PWM Technique in Series Connected Voltage Inverters", N Y USA.
- [5] Atmel Corporation 2000, AT89C51 Microcontroller Datasheet.
- [6] National Semiconductor, DAC 0808 (8 bit D/A Converter) Datasheet.
- [7] A. Tahri, A. Draou and M. Ermis, "A Comparative Study of PWM Control Techniques for Multilevel Cascaded Inverters," Applied Power Electronics Laboratory, Department of Electrotechnics, University of Sciences and Technology of Oran, BP 1505 El Mnaour (31000 Oran), ALGERIA.
- [8] N.A. Rahim (Member IEEE), E.A.Mahrous, K.M.Sor(Senior Member IEEE), "Modeling And Simulation of Linear Generator PWM Multilevel Inverter", National Power and Energy Conference (PECon) 2003 Proceedings , Malaysia.
- [9] Leon M Tolbert (Oak Ridge National Laboratory), Thomas .G.Habetler (Georgia Institute of Technology, School of Electrical and Computer Engineering, Atlanta),
"Novel Multilevel Inverter Carrier Based PWM Method".
- [10] G. Sinha, T.A.Lipo, "A Four Level Rectifier Inverter System for Drive Applications", IEEE IAS Annual Meeting 1996, pp 980-987
- [11] G.Carrara, D.Casini, S.Gardella, R.Salutari, "Optimal PWM for the Control of Multilevel Voltage Source Inverter", Fifth Annual European Conference on Power Electronics , volume 4 ,1993 ,pp255-259