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Closed Loop Controlled Hybrid Boost Three Level DC-DC Converter with High Voltage Gain for PV Systems

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Abstract:

To overcome the problem of mismatched voltage levels between parallel-connected low voltage photovoltaic (PV) arrays and the higher grid voltage, a hybrid boost three level dc-dc converter is developed based on three level inverter with the traditional single phase diode clamping. Only one inductor, two capacitors in series, and those power switches and diodes, which are easy to be integrated, are used for establish the topology with transformerless high voltage gain. The operation principle of the topology is analyzed, and then the pulse width modulation (PWM) control method is obtained according to the switching functions about the output pulse voltages of both half-bridges. Therefore, the converter can not only operate with high voltage gain, but also make the duty cycles of power switches closer to 0.5. A feedforward closed loop control operation is proposed such that even in varying input the converter is capable of giving a constant output. Finally an experimental is set up in the laboratory for open loop control operation. All experimental results verify the feasibility of the circuit and validity of the PWM control method.

Keywords- ***Photovoltaic system(PV system), Hybrid boost converter***

I. INTRODUCTION

Both photovoltaic (PV) and wind power generations have become important parts of renewable energy sources, due to worldwide exhausted fossil fuel and worlds demand for clean energy. In grid-connected PV generation systems, a single PV array can only supply lower dc voltage, but higher voltage level is demanded for the grid-connected side. Therefore, the mode of PV arrays in series has been adopted to offset the differential voltage levels between dc bus and grid side. Unfortunately, low voltage PV arrays are always subjected to inevitable cloud, dust, shadow, and so on, which will limit the output current of the total PV arrays, and then the efficiency of the entire PV generation system will be degraded. Naturally, the other mode of PV arrays in parallel has also been proposed, and the power generation level can be improved by extending the parallel connected PV arrays flexibly.

Considering parallel connected PV configuration, the most important problem is that the low dc bus voltage has to be boosted to high voltage. Therefore, high step-up dc-dc converters are introduced between low voltage parallel connected PV arrays and the demanded high voltage grid connected side for the voltage conversion. When converters operate with high step-up gains, high output voltage would be sustained completely by the power switches in conventional boost two-level converters. The classical boost three-level converters could reduce half of the voltage stress, but it requires extreme duty cycles of power switches which limits its voltage gains and switching frequency because of the shorter turn off time of the power switches in each switching period.[1]-[3]

Cascaded boost converters are also used to extend the voltage gain and duty cycles, but one obvious disadvantage is that it requires more number of separate inductors, and the power switch of the last power stage cannot avoid the output voltage stress. Many researchers have put their studies on step-up converters with coupled inductor in recent years, which has the transformer function to extend the voltage gain and duty cycles. Although the voltage stress of power switches is low, the output power level is limited and the input current ripple is large due to the single phase structure. Therefore, the idea of interleaved boost converters with switched capacitors came into being. However, more switched capacitor cells are required to obtain a high voltage gain. An interleaved high step-up converter integrated with winding-cross-coupled inductors and voltage multiplier cells is presented, but it sponges on more coupled inductors which are not easy to be integrated or designed in standardization. In addition, the duty cycles of the power switches inclines to 1, due to the increased voltage gain.[4]-[7]

A hybrid boost three-level dc-dc converter with closed loop control is proposed in this project, taking the topology established without a transformer or coupled inductors into account. It is composed of only one inductor, two output capacitors in series, and other power semiconductor components, which are easy to be integrated. This converter can not only realize high step-up gain, but also avoid extreme duty cycles. The deduction of the topology synthesis with closed loop control is explained in this project and simulation results are obtained. Also, a prototype is set up for the open loop control, and the effective experimental results are obtained.

II. HYBRID BOOST THREE LEVEL DC-DC CONVERTER

This topology mainly consists of 4 control switches. The interleaved conduction property and hybrid switching property are clubbed together here. Apart from the control switches, the circuit requires 8 diodes. Also, a boost inductor and 2 output capacitors in series are implemented in the circuit.

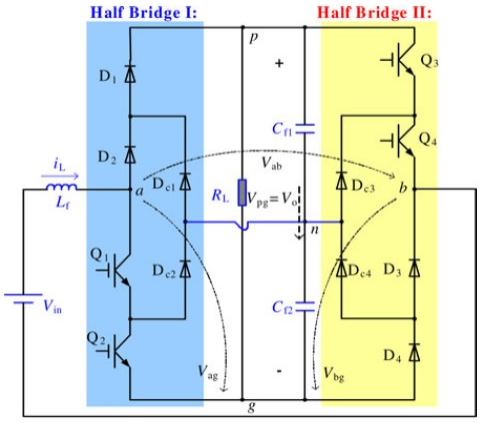


Fig. 1 Hybrid Boost Three Level DC-DC Converter

Fig. 1 shows the circuit diagram. As already mentioned, there are 4 control switches Q_1 - Q_4, 8 diodes D_1 - D_4 and D_{c1} - D_{c4}, 2 output capacitors C_{f1} and C_{f2} and the boost inductor L_f . As shown in the figure, it is basically an interconnected circuit with two half bridges with hybrid switching. In this way the interleaved conduction property can be implemented. If the half bridges are operated individually, each requires a separate inductor and 2 capacitors; on a whole 2 inductors and 4 capacitors would be required. Additional advantage of the interconnection is that a single inductor and 2 capacitors can be shared by both the half bridges. Consider the points a, b, p and g shown in the Fig.1. g is the ground terminal taken for the load R_L. The output of half bridge I is voltage across a and g, V_{ag}. The output of half bridge II is across b and g, V_{bg}. Thus the resultant of these outputs of half bridges acts as an output voltage pulse V_{ab} across the load.

$$V_{ab} = V_{ag} - V_{bg}$$

The capacitors C_{f1} and C_{f2} filter this output voltage pulse and generates constant DC voltage across the load, $V_o = V_{pg}$. Values

of the capacitors determine the voltage ripple in the output DC voltage.

A. MODES OF OPERATION

The modes of operation can be explained by considering the switching of control switches and its consequences. For a particular switching frequency, switches Q_1 and Q_2 are operated for first half cycle, and, switches Q_1 and Q_2 are operated for second half cycle. Pulse width of gate signal to Q_1 is greater than that to Q_2. Similarly, pulse width of gate signal to Q_4 is greater than that to Q_3. Switches Q_1 and Q_4 are complementary, ie., they operate with same pulse width but in different half cycles. Same is the case for Q_2 and Q_3. Based on the switching states, there are 5 modes of operation for the circuit. Fig.2 shows the mode of operation, in which the waveforms of the gate signals to the switches and corresponding change in V_{ag}, V_{bg} and V_{ab} are shown.

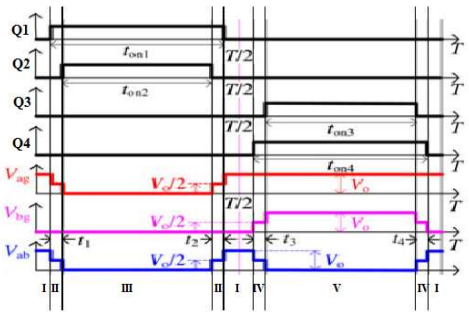


Fig. 2 Modes of Operation

1) Mode I: In this mode, all the control switches will be switched off. Diodes D_1 - D_4 will be in conduction. The inductor is discharging and both the capacitors are charging. In a single period of gate signal, this mode occurs in three times. Here, $V_{ag} = V_o$, $V_{bg} = 0$, and $V_{ab} = V_{ag} - V_{bg} = V_o$. Fig. 3(a) shows the region of operation where unshaded portion represents the region. Fig. 3(b) shows the current flow in the circuit.

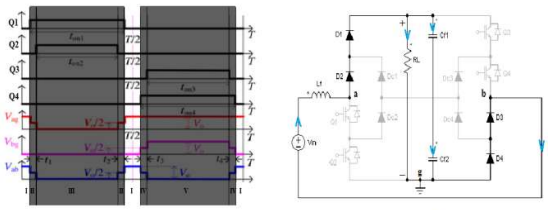


Fig. 3 Mode I (a) Region of Operation (b) Current Flow Diagram

2) Mode II: In mode II operation, Q_1 is switched on. Diodes D_{c2}, D_3 and D_4 will be conducting. This mode operates in the first half cycle. The inductor is discharging. Capacitor C_{f1} is discharging and Capacitor C_{f1} is charging. Half bridge outputs, $V_{ag} = V_o/2$, $V_{bg} = 0$, and $V_{ab} = V_o/2$. Fig. 4 shows the mode II operation.

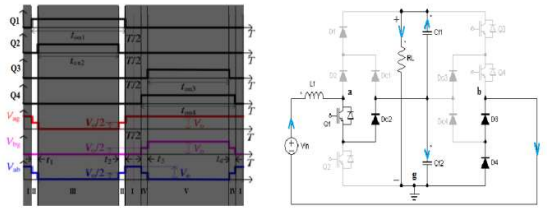


Fig. 4 Mode II (a) Region of Operation (b) Current Flow Diagram

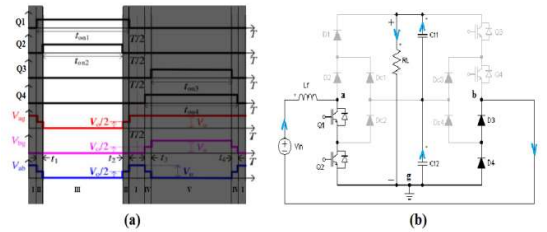


Fig. 5 Mode III (a) Region of Operation (b) Current Flow Diagram

3) Mode III: In mode III operation, Q_1 and Q_2 are switched on. Diodes D_3 and D_4 will be conducting. The inductor is charging and the output voltage to the load is supplied by discharging the capacitors. $V_{ag} = 0$, $V_{bg} = 0$, and $V_{ab} = 0$. Fig. 5 shows the mode III operation.

4) Mode IV: Mode IV is a complementary action of mode II, which operates in the other half cycle. Here Q_4 is switched on. Diodes D_{c3}, D_1 and D_2 will be conducting. The

inductor is discharging, C_{f1} is charging and C_{f2} is discharging. $V_{ag} = V_o$, $V_{bg} = V_o/2$, and $V_{ab} = V_o/2$. Fig. 6 shows the mode IV operation.

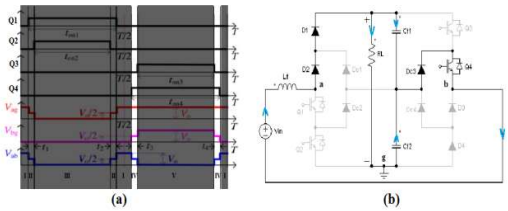


Fig. 6 Mode IV (a) Region of Operation (b) Current Flow Diagram

5) Mode V: As in the previous case, mode V is a complementary action of mode III operation in the other half cycle. Q_3 and Q_4 are switched on. Diodes D_1 and D_2 will be conducting. The inductor is charging and the output voltage to the load is supplied by discharging the capacitors. $V_{ag} = V_o$, $V_{bg} = V_o$, and $V_{ab} = 0$. Fig. 5 shows the mode V operation.

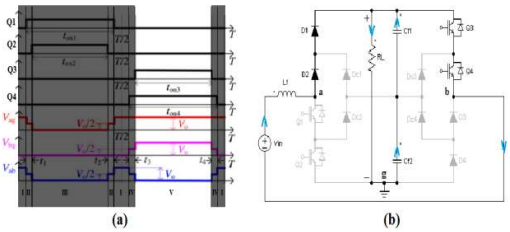


Fig. 7 Mode V (a) Region of Operation (b) Current Flow Diagram

B. VOLTAGE GAIN EQUATION

The voltage gain equation is derived with the help of the energy balance equation of the inductor. Consider the operating modes waveforms in fig. 2. t_{on1}, t_{on2}, t_{on3} and t_{on4} are the turn on time periods of switches Q_1, Q_2, Q_3 and Q_4 respectively. d_1, d_2, d_3 and d_4 are the corresponding duty ratios. As mode II and IV, and, mode III and V are complementary, $t_{on1} = t_{on4}$ ($d_1 = d_4$) and $t_{on2} = t_{on3}$ ($d_2 = d_3$). T is the total time period. I_L is the average inductor current.

The energy stored in the inductor,

$$W_{st} = V_{in} \times I_L \times t_{on2} \times 2$$

(by considering complementary actions in the total time period, equation in mode I is doubled)

The energy transferred from the inductor,

$$W_{tr} = (V_o - V_{in}) \times I_L \times \left(\frac{T}{2} - t_{on1}\right) \times 2 + \left(\frac{V_o}{2} - V_{in}\right) \times I_L \times (t_1 + t_2) \times 2$$

where,

$$(t_1 + t_2) = (t_{on1} - t_{on2})$$

Assuming the ideal case, energy transferred from the inductor will be equal to the energy stored in it.

$$W_{st} = W_{tr}$$

Putting these equations together,

$$\frac{V_o}{V_{in}} = \frac{T}{T - (t_{on1} + t_{on2})}$$

But $t_{on1} = d_1.T$ and $t_{on2} = d_2.T$. And also, voltage gain $M = V_o/V_{in}$. Therefore,

$$M = \frac{1}{1 - (d_1 + d_2)}$$

From the above equation, it is clear that extreme duty cycle for the switches are not needed for high voltage gain, it can be obtained from duty ratios close to 0.5. The equation shows that at 0.5 duty ratio, the gain will be infinity.

IV. CLOSED LOOP CONTROL

For a given input, the required output can be obtained by switching with particular duty cycles. This is the open loop control. But for PV systems, input is always varying as the intensity of sunlight varies continuously. So open loop control is not reliable, closed loop control is required to obtain constant output even if the input is varying. This section explains about a closed loop control for the hybrid boost three level DC-DC converter.

A. PWM STRATEGY

The basic idea for the closed loop control implemented here is that changing the gain value for varying inputs to obtain a constant output. For that, duty cycles of the switching pulses are varied according to the change in input voltage. As there are 4 different gate signals, 4 different calculations are required from a single value. For that, a specific PWM strategy is proposed and it is explained below.

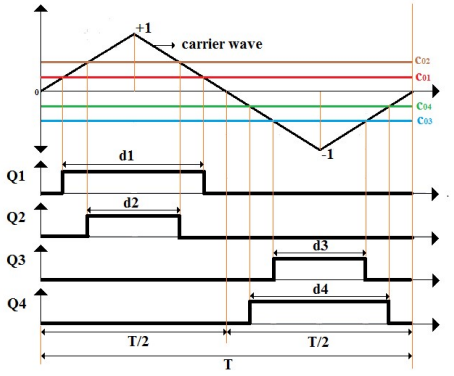


Fig. 8 PWM Strategy

Fig. 8 shows the PWM strategy. For making the calculations simple, the carrierwave taken is a triangular wave with peak amplitudes +1 and -1. d_1, d_2, d_3 and d_4 are the duty cycles of Q_1, Q_2, Q_3 and Q_4 respectively. For obtaining these gate signals, the carrier wave is compared with constant values c_{01}, c_{02}, c_{03} and c_{04} as shown in the figure. For making d_1 - d_4 and d_2 - d_3 pairs complementary, c_{01} and c_{04} are equal values having opposite signs; same is the case for c_{02} - c_{03}. When magnitude of carrierwave is greater than c_{01} and c_{04}, gate signals for Q_1 and Q_4 are generated. When magnitude of carrierwave is less than c_{02} and c_{03}, gate signals for Q_2 and Q_3 are generated, for giving a 180 degree shift.

From the figure it is found that,

$$d_1 = 0.5 - (0.5 \times c_{01})$$
$$d_4 = 0.5 + (0.5 \times c_{04})$$

The 4 gate signals must be generated with a single value control, say 'c', for reliable operation. For that the 4 constants c_{01}, c_{02}, c_{03} and c_{04} must be given in terms of c. Assume c_{02} = c and c_{01} = 0.5c, c_{03} = -c and c_{04} = -0.5c. So the above equations changes to,

$$d_1 = 0.5 - (0.25 \times c)$$
$$d_4 = 0.5 - (0.25 \times c)$$

Then the equation for voltage gain changes to,

$$M = \frac{1}{1 - (d_1 + d_2)}$$
$$= \frac{1}{1 - \{0.5 - (0.25 \times c) + 0.5 - (0.5 \times c)\}}$$
$$= \frac{4}{3c}$$

The above equation shows that the voltage gain M can be adjusted by controlling single value c, instead of adjusting the 4 gate signals separately. Here a carrierwave of peak +1 and -1 is taken. Practically it is available with logic 0 and 1 (0V and +5V). To consider these changes, the carrier waveform shown in figure 4.1 has to be proportionally shifted upwards to make the peak points 0 and +5. Then c_{01}, c_{02}, c_{03} and c_{04} to c_1, c_2, c_3 and c_4 as given below,

$$c_1 = 2.5 + (1.25 \times c)$$
$$c_4 = 2.5 - (1.25 \times c)$$

Only the relation between c and individual constants changes due to proportional shifting. The voltage gain equation remains same, M = 4/(3c). For closed loop control, a relation between c and Vin has to be found. Looking into the gain equation,

$$M = \frac{4}{3c}$$

where k = 4/(3Vo). As output voltage has to be taken as constant, value of k will be constant. Thus a linear relationship between c and Vin is obtained. For the variations in input voltage, control can be implemented in this converter using this equation to get a constant output. Here ideal case is taken and a linear relationship between c and V_{in} with origin 0 is obtained. In practical case, the equation will have an additional intercept value.

V. SIMULATION MODEL AND RESULTS

Simulation is done for both open loop and closed loop control. It is done with practical settings to get an idea of variation in ideal theoretical concepts and practical scenario. IGBTs are the controlled switches used for the simulation. For the open loop control, a PV system with 50V is taken as input. The converter has to boost it to 600V (M = 12). Maximum inductor current through the inductor is 50A. Load is 1k resistor. Switching frequency taken is 5kHz.

Voltage gain M = 12, so constant c is,

$$c = \frac{4}{3 \times c} = \frac{4}{3 \times 12} = \frac{1}{9}$$

Taking current ripple, ΔI_L in the inductor as 7% of inductor current,

$$\Delta I_L = 0.07 \times I_L = 0.07 \times 50 = 3.5A$$

Taking output ripple, ΔV_o as 2% of output voltage,

$$\Delta V_o = 0.02 \times V_o = 0.02 \times 600 = 12V$$

Output current, I_o is,

$$I_o = \frac{V_o}{R_L} = \frac{600}{1000} = 0.6A$$

For a boost converter, design equation for the boost inductor L_f is,

$$L_f = \frac{V_{in}(V_0 - V_{in})}{\Delta I_L \times f_s \times V_o} = \frac{50(600 - 50)}{3.5 \times 5000 \times 600} = 2.6mH$$

The effective duty cycle for the converter, D is,

$$D = 1 - \frac{1}{M} = 1 - \frac{1}{12} = 0.9167$$

The output filter capacitor value, C_f is,

$$C_f = \frac{I_o \times D}{f_s \times \Delta V_o} = \frac{0.6 \times 0.9167}{5000 \times 12} = 9.2\mu F$$

For the simulation model, round of values L_f = 5mA and C_f = 11μF (C_{f1} = C_{f2} = 22μF) are taken. The simulation parameters are shown in table 1.

TABLE 1
Simulation Parameters

Input Voltage, Vin	50V
Output Voltage, Vo	600V
Voltage Gain, M	12
Load, RL	1kΩ
Maximum Inductor Current, Il	50A
Switching Frequency, fs	5kHz
c	1\9
Boost Inductor, Lf	5mH
Output Capacitors, Cf1 = Cf2	22μF

The simulation diagram with the design values is shown in fig. 9 with the PWM strategy explained in last session. The waveforms of output voltage and inductor current is shown in fig. 10. The circuit was designed for 600V with ideal scenario but simulation results with settings of practical scenario shows an output of 578V. So the efficiency is η = 578/600 = 96.33%. The maximum inductor current taken for design was 50A and simulation result shows the steady-state inductor current around 25A. So it is under the limit. Waveforms of the half bridge output voltages V_{ag} and V_{bg}, and the output voltage pulse V_{ab} are shown in fig. 11. Each waveform has three levels of 0, $V_o/2$ and V_o.

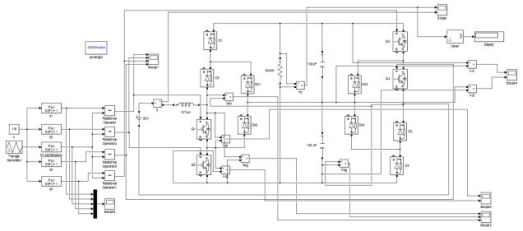


Fig. 9 Simulation Model for Open Loop Control

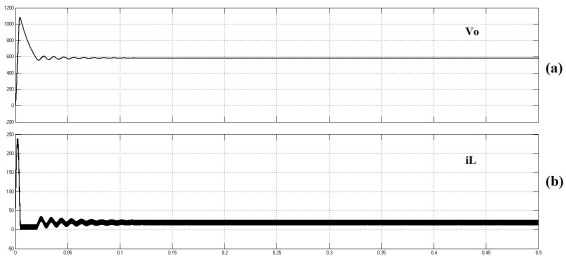


Fig. 10 (a)Output Voltage V_o (b) Inductor current I_L

The closed loop control is designed for 600V output voltage. Fig. 12 shows the variation made in c for different inputs to make the output at 600V in open loop control. It can be seen that there is a linear relationship between c and V_{in}. By verifying the axes points, equation for this linear relationship is,

$$c = 0.0022V_{in} - 0.0038$$

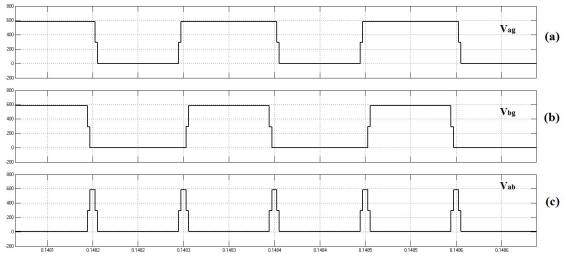
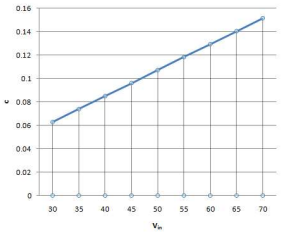


Fig. 11 Half Bridge Outputs and Output Voltage Pulse (a) V_{ag} (b) V_{bg} (c) V_{ab}

This equation is used for closed loop control. Figure 5.13 shows the simulation diagram for closed loop control. The simulation parameters are taken as same as that of open loop control, except the input voltage is switched alternatively at different intervals for showing the variation in input. Fig.14 shows the switching sequence for the input. The gate circuit for closed loop control is shown in fig. 15 V_{in} is taken and converted to c value. c is again converted to individual constant values c_1, c_2, c_3 and c_4. Then these values are compared with amplitude of carrierwave signal to generate various gate signals. As the input voltage changes, duty cycle of gate pulses change accordingly. Fig. 16 shows waveforms for V_{in}, V_o and inductor current I_L. Input voltage is varied from 40V to 50V and finally to 60V. In all cases, after some distortion in transient state, the value settles to 600V in steady state.

Vin	c
30	0.0628
35	0.0739
40	0.085
45	0.0961
50	0.1072
55	0.1183
60	0.1294
65	0.1405
70	0.1516

(a)



(b)

Fig. 12 (a) Table for V_{in} vs c (b) Graph showing Linear Relationship

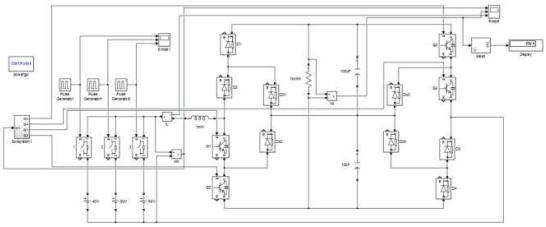


Fig. 13 Simulation Diagram for Closed Loop Control

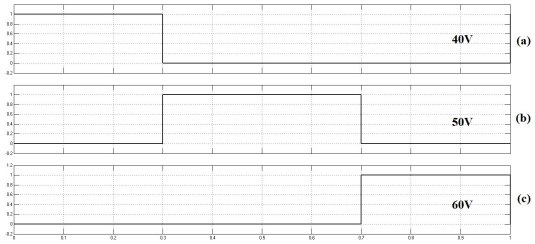


Fig. 14 Switching Sequence for Input Voltages

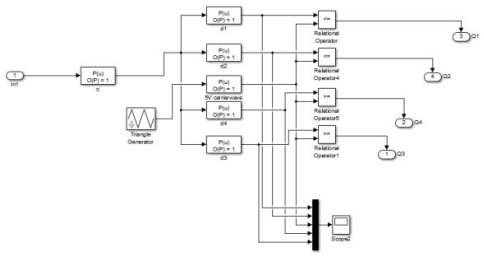


Fig. 15 Gate Circuit for Closed Loop Control

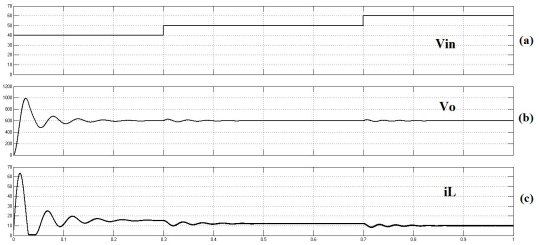


Fig.16 Closed Loop Control (a) Input Voltage V_{in} (b) Output Voltage V_o (c) Inductor Current I_L

VI. HARDWARE IMPLEMENTATION

The laboratory hardware testing is done for the open loop control. Fig.17 shows the prototype. The input is 5V and output is 33.33V. Since it is a low power circuit, low rating MOSFETs IRF 540 are taken as controlled switches. The switching frequency is 5kHz. PIC 16F877A is programmed to generate the gate pulses to have voltage gain M = 20/3(this value was chosen as it is easy to program the corresponding gate pulses). The diodes are fast recovery diodes 1N4148. Converter circuit capacitors and inductor are chosen as per design values. Fig. 18 shows the input and output voltage waveform. Input was regulated DC voltage taken from AC mains using regulator IC 7805 and 4.92V DC was generated which is near to 5V. For this input a satisfactory output of 18.6V DC was obtained. This difference in practical value is due to the fact that there will be unavoidable circuit resistance drops and it also leads to unbalance in charging and discharging of the two capacitors. When the circuit is of low power, these errors become prominent. The efficiency was found to be 56%. Fig. 19 shows the three level operation. 19(a) shows waveform of V_{ag} and V_{bg}, the output voltages of half bridges I and II respectively. Pulse V_{bg} is shorter width than V_{ag}. 19(b) shows V_{ab}, the output voltage pulse, which is the difference of V_{ag} and V_{bg}.

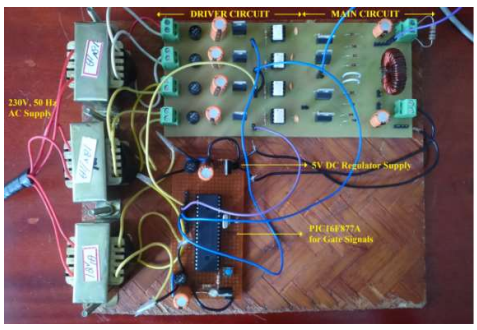
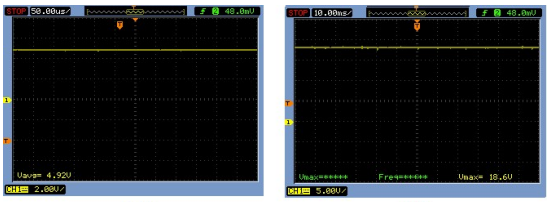
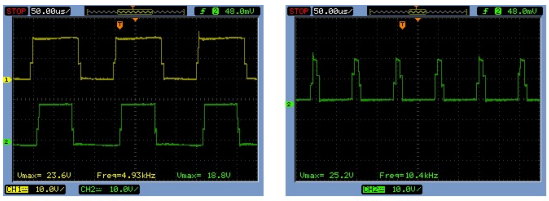


Fig. 17 Experimental Setup



(a) (b)

Fig.18 (a)V_{in} (b)V_o



(a) (b)

Fig. 19 (a)V_{ag} and V_{bg} (b)V_{ab}

VII. CONCLUSIONS

The hybrid boost three-level DC-DC converter is explained in this paper, based on the conventional single-phase diode clamped three-level inverter. It can not only operate with transformerless high voltage gain, but also make the duty cycles of the power switches closer to 0.5 with the increasing voltage gain, instead of the extreme duty cycles. Moreover, a flexible PWM switching strategy and closed loop control is explained. In the simulation of open loop control, circuit was designed to give an output of 600V for 50V input taking the ideal case. Simulation result shows an output of 578V, with an efficiency of 96.33. For the simulation of closed loop control, the switching pulse width is varied with change in input voltage to obtain a constant voltage. Simulation for closed loop control operation with input range 30V - 70V and output 600V has been done. It was observed that when there is abrupt change in input, after some distortion in the transient state, the output voltage settles to a constant value in steady state. Laboratory experiment of the circuit with open loop control has been done. The circuit was designed for a gain of M = 20/3. For an input of 4.92V, the output was 18.6V with around 56% efficiency. So the efficiency will be higher for higher voltage levels as there will be unavoidable circuit resistance drops and it also leads to unbalance in charging and

discharging of the two capacitors and for the low power circuit, these errors become prominent.

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