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Experimental Analysis of the Variants of UBCT Amplifier Circuit

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Abstract:

The Unipolar-Bipolar Composite Transistor (UBCT) circuit is designed to combine the advantages of high input resistance of unipolar transistor and transfer curve linearity of bipolar transistor. The Composite Circuit has been designed with n-channel JFET, npn BJT and a pair of resistors, therefore, this type of JFET-BJT composite transistor is classified as UBCT. This UBCT circuit exhibits enhanced static and dynamic performances as compared to that of JFET. In the present correspondence, the performances of the variants of the UBCT amplifier circuit have been experimentally analysed on the basis of power dissipation level and the corresponding voltage gain of the amplifier. According to the experimental results, the UBCT amplifier circuit can be used as a power efficient small signal amplifier for analog applications.

Keywords - Composite Transistor, CT, Unipolar-Bipolar Composite Transistor, UBCT, JFET-BJT Composite Transistor, M-FET, UBCT Amplifier

I. INTRODUCTION

The Unipolar-Bipolar Composite Transistor (UBCT) consists of circuit combination of Unipolar (JFET) and Bipolar (BJT) active components in association with resistive passive components. The resultant circuit design can be considered for fabrication as a single equivalent transistor, hence it is categorised as Composite Transistor (CT). The primary motive behind designing the circuit for UBCT is to utilize the advantages of high input resistance of JFET along with linear transfer characteristics of BJT. Thus, these JFET and BJT devices are designed in combination to achieve better performance that can be obtained with either active device alone [1]. The JFET-BJT composite transistor circuit was introduced by Mylroie in 1979 [2]. Later in 1985, the BJTs were started to be fabricated along with thin implanted JFETs on the same chip to create BIFET structure in Monolithic Integrated Circuit (MIC) technology [3].

The JFET-BJT combination having FET like characteristic has been reported in early literature, which comprises an n-channel JFET and a pnp BJT along with three resistors. It offers high input resistance and widespread linear transfer characteristics [4]. Later, this composite transistor is further thermally improved by comprising of an n-channel JFET, four npn BJTs, a pnp BJT and three resistors [5]. Due to its improved FET like characteristics, it is designated as "Modified Field Effect Transistor (M-FET)". The M-FET has marked improvement in the transfer curve linearity associated with good thermal stability [6]. Since it exhibits superior performances to that of JFET, hence this JFET-BJT composite transistor finds better applications in designing amplifiers and oscillators [7].

II. CIRCUIT DESIGN OF UBCT

The circuit of UBCT has been designed with n-channel JFET (BFW10), npn BJT (CL100) and a pair of source and emitter resistors (R_S-R_E). The drain of JFET and collector of BJT are connected together to form final drain, base is connected to the source, and emitter and source are connected in series with the emitter resistor and source resistor respectively to form the final source for the UBCT.

The gate of JFET works as well as the final gate for UBCT. According to this UBCT circuit topology, it can also be fabricated by BIFET MIC technology and designated as a three terminal composite transistor device as depicted in fig.1.

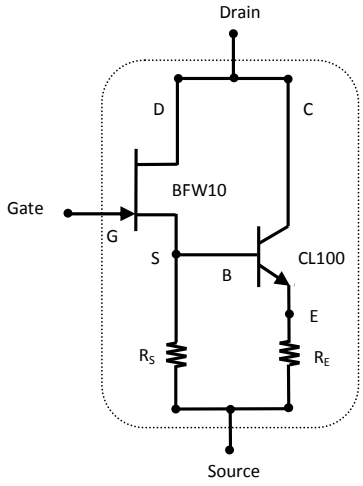

Fig.1 Circuit design of UBCT
(JFET-BJT Composite Transistor)
JFET BFW10, BJT CL100, (R_S-R_E) Resistor pair

This type of UBCT is specifically considered as a simplified circuit design of earlier reported JFET-BJT composite transistors [8]. The circuit components of UBCT (JFET-BJT composite transistor) have been optimized for parametric enhancement [9]. According to the static performance, it also offers wide range linearity in transfer curve and very high input resistance [10]. The drain resistance and transconductance curves also exhibit linearity over the wide range of drain-to-source voltage and gate-to-source voltage respectively up to the pinch-off value of UBCT [11]. The dynamic performance of UBCT circuit promotes its application as an efficient small signal amplifier [12].

III. UBCT AMPLIFIER CIRCUIT

This UBCT is used as an active component in a common source amplifier circuit as depicted in fig.2. The circuit is biased under the source self-biasing topology of JFET amplifier with an applied ac source capacitively coupled to the gate input. The output of the amplifier is obtained at the drain end of the UBCT. The source self-biasing or self-biasing is basically a current series feedback circuit in which the source feedback resistor R_{S1} is used to provide Q-point stabilization against change in transistor parameters and variation in temperature.

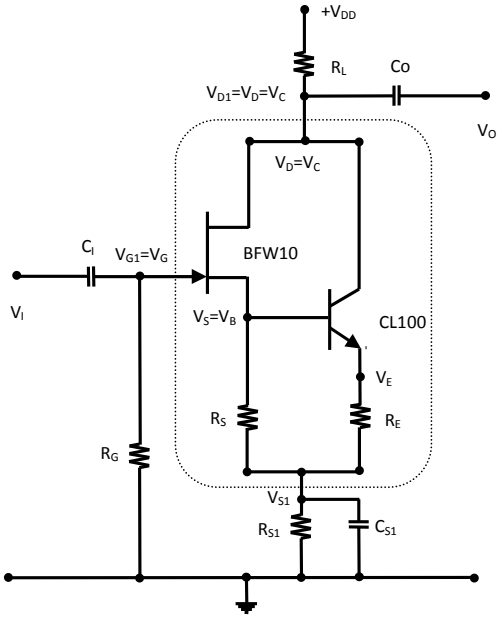

Fig.2 Circuit design of UBCT Amplifier

The feedback voltage is developed across source resistor R_{S1} and the negative feedback can also be invalidated by using the source bypass capacitor C_{S1}, which keeps the source of the UBCT effectively at ac ground [13]. The gate resistor R_G can be large, usually of 1MΩ, which serves to maintain the average gate voltage at ac ground [14]. Also the large value of R_G prevents loading of the ac signal source. The passive circuit components used in UBCT amplifier e.g. the resistors and capacitors along with the operating supply voltage have been optimized by a sequence of different sets of experimental observations for procurement of possible parametric boosts. The experimental results confirm that passive components have been optimized at their standard values e.g. the load resistor R_L=1kΩ, gate resistor R_G=1MΩ, source resistor R_{S1}=100Ω, input & output coupling capacitors C_I=C_O=10μF, source bypass capacitor

C_{S1}=N/C for providing voltage gain with negative feedback and the supply voltage V_{DD} =18V within the operating temperature range of 32°C to 35°C.

IV. EXPERIMENTAL ANALYSIS

For experimental analysis of the variants of UBCT amplifier circuit, ac experiments have been performed in which the effects of supply voltage and the corresponding power dissipation level on the voltage gain of the UBCT amplifier are precisely studied.

(A) Supply Voltage Analysis for UBCT Amplifier Circuit

The experimental observations have been taken for five variants of UBCT amplifier circuit having different resistor pairs (R_S-R_E) (10kΩ-1kΩ), (1kΩ-1kΩ), (1kΩ-100Ω), (100Ω-100Ω) and (100Ω-10Ω) with the supply voltage ranging from 9V to 24V DC and input ac voltage of 100mV (peak-to-peak) having constant frequency of 1 kHz (sine wave). These observations are plotted in the graph shown in fig. 3.

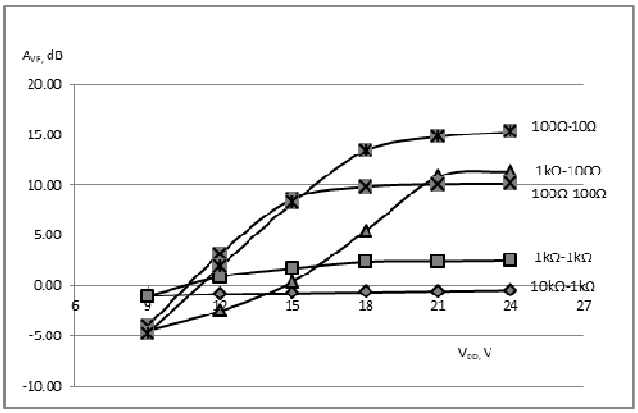

Fig.3 Voltage gain with negative feedback A_{VF} versus the supply voltage V_{DD} for the variants of UBCT Amplifier circuit having five different resistor pairs (R_S-R_E).

Specifications: UBCT (JFET BFW10, BJT CL100, resistor pair R_S-R_E), R_L=1kΩ, R_G=1MΩ, R_{S1}=100Ω, C_I=C_O=10μF, C_{S1}= N/C in case of negative feedback, T=32-35°C, input ac voltage V_I =100 mV (p-p) of 1 kHz.

Based on the experimental observations, it appears that the variants having resistor pair (R_S-R_E) (100Ω-10Ω) as well as (100Ω-100Ω) should be better choice as the voltage gain A_{VF} of about 8dB has been achieved even at lower supply voltage V_{DD}=15V. At V_{DD}=21V & 24V, the variant having resistor pair (R_S-R_E) (1kΩ-100Ω) also shows better voltage gain. The UBCT variants having resistor pair (R_S-R_E) (10kΩ-1kΩ) and (1kΩ-1kΩ) do not show considerable voltage gain for the entire experimental range of supply voltage from 9V to 24V. The supply voltage V_{DD}=21V and above, the voltage gains for all the resistor pair (R_S-R_E) are almost about to be saturated. In these observations, the variant of UBCT amplifier circuit having resistor pair (R_S-R_E) (100Ω-10Ω) exhibits the best performance as the voltage gain A_{VF} of 13.39dB is achieved at the supply voltage V_{DD} =18V.

(B) Power Dissipation Analysis for UBCT Amplifier Circuit

The objective of power dissipation analysis is to design a power efficient UBCT amplifier circuit which offers the best possible voltage gain at the optimal power dissipation level. The experimental observations for the analysis of power dissipation of UBCT amplifier are plotted in the column graph as shown in fig. 4. The graph depicts the Voltage gain with negative feedback, Total power dissipation of the circuit, power dissipation across Load resistor, UBCT, JFET and BJT respectively for five variants of UBCT circuits consisting of different pairs of source and emitter resistors (R_S-R_E) having values (10kΩ-1kΩ), (1kΩ-1kΩ), (1kΩ-100Ω), (100Ω-100Ω) and (100Ω-10Ω) at constant supply voltage V_{DD} of 18V. The supply voltage of V_{DD} = 18V is optimized because the voltage gains of four out of five variants of UBCT have been almost saturated. The power dissipation observations display that the obtained voltage gains for different resistor pairs (R_S-R_E) (10kΩ-1kΩ), (1kΩ-1kΩ), (1kΩ-100Ω), (100Ω-100Ω) and (100Ω-10Ω) are -0.63dB, 1.87dB, 5.44dB, 9.54dB and 13.39dB respectively. In view of this, use of the variants of UBCT having resistor pairs (R_S-R_E) (10kΩ-1kΩ) and (1kΩ-1kΩ) are avoided and not to be considered because of their lower voltage gains. The variant of UBCT having resistor pair (R_S-R_E) (1kΩ-100Ω) also gives a lower

voltage gain of 5.44dB with a large total power dissipation level of 242.28mW. The satisfactory results have been obtained by the use of the variants of UBCT having resistor pairs (R_S-R_E) (100Ω-100Ω) and (100Ω-10Ω) with better voltage gain of 9.54dB and 13.39dB at comparable lower power dissipation level of about 158.58mW and 203.58mW respectively. Overall, the best result is offered by the variant of UBCT having resistor pair (R_S-R_E) (100Ω-10Ω) as compared to that of (100Ω-100Ω) is due to the optimal power dissipation levels of load resistor, UBCT, JFET and BJT.

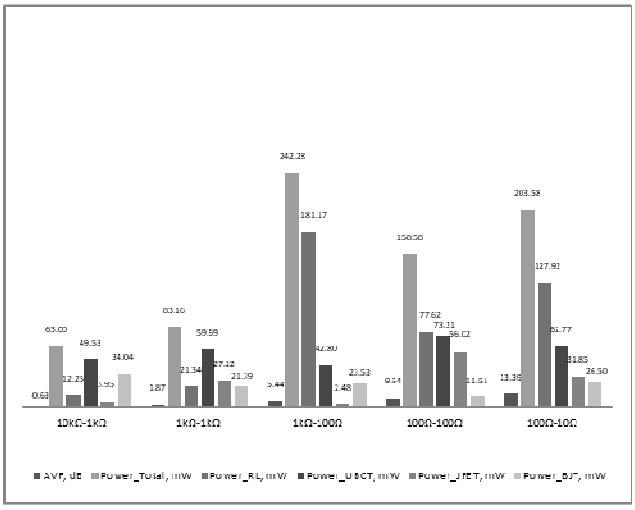

Fig.4 Power Dissipation level of the variants of UBCT Amplifier circuit having five different resistor pairs (R_S-R_E).

Specifications: UBCT (JFET BFW10, BJT CL100, resistor pair R_S-R_E), R_L=1kΩ, R_G=1MΩ, R_{S1}=100Ω, C_I=C_O=10μF, C_{S1}= N/C in case of negative feedback, T=32-35°C, input ac voltage V_I =100 mV (p-p) of 1 kHz at a constant supply voltage V_{DD}=18V.

V. CONCLUSION

The present paper represents the experimental analysis regarding the performance of the variants of UBCT amplifier circuit. Observations for these variants have been studied precisely by keeping some parameters constant during the experiment e.g. the supply voltage V_{DD} is kept constant at 18V, the input ac voltage V_I=100mV (p-p) of 1kHz, load resistor R_L=1kΩ, source resistor R_{S1}=100Ω, gate resistor R_G=1MΩ, input & output coupling capacitors C_I=C_O=10μF, source bypass capacitor C_{S1}=N/C for providing voltage gain with negative feedback and the range of operating temperature is between 32°C to 35°C. According to the experimental observations, the UBCT amplifier circuit having resistor pair (R_S-R_E) (100Ω-10Ω) has performed the best among all other variants as it could be able to deliver the voltage gain of 13.39dB at total power dissipation level of 203.58mW. At this condition, the power dissipation levels of the UBCT, JFET and BJT are 62.77mW, 31.85 mW and 26.50mW respectively, whereas the power dissipation level of the load resistor is 127.92mW. Since all these power dissipation levels are in safe region as per the data sheets of the components used in the circuit, hence the designed UBCT amplifier circuit can be used as a power efficient small signal amplifier for analog applications.

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