RESEARCH ARTICLE OPEN ACCESS

HIGH EFFICIENCY ELECTRIC VEHICLE BATTERY CHARGING SYSTEM USING MCPWM AND PSO TECHNIQUE

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Abstract:

The charger plays a very important role within the development of electrical vehicles (EVs) and plug-in hybrid electrical vehicles (PHEVs).This thesis focuses on the DC-DC device for prime voltage charger and is split into four chapters. The background associated with EV battery charger is introduced, and therefore the topologies of isolated DCDC device presumably applied in battery charge square measure sketched in Chapter one. Since the EV charger is high voltage high power, the phase-shifted full bridge and LLC converters, that square measure popularly utilized in high power applications, square measure mentioned intimately in Chapter two. The typically thought-about as high efficiency, high power density and high dependability, however their distinguished options are restricted in sure vary of operation. to form full use of the benefits and to avoid the limitation of the phase-shifted full bridge and LLC converters, a completely unique hybrid resonant and PWM device combining resonant LLC half-bridge and section shifted full-bridge topology is projected and is described in Chapter three. The device achieves high potency and true soft switch for operation vary, that is incredibly necessary for prime voltage EV charger application.

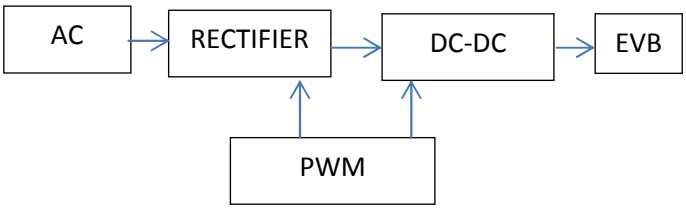
I.INTRODUCTION

To make full use of the benefits and to avoid the limitation of the phase-shifted full bridge and LLC converters, a completely unique hybrid resonant and PWM device combining resonant LLC half-bridge and section shifted full-bridge topology is planned. The device achieves high potency and true soft change for the complete operation vary, that is incredibly vital for top voltage energy unit charger application. A 3.4 kilowatt hardware paradigm has been designed, enforced and tested to verify that the planned hybrid device really avoids the disadvantages of LLC and phase-shifted full bridge converters whereas maintaining their benefits. During this planned hybrid device, the employment potency of the auxiliary electrical device isn't that ideal. once the duty cycle is giant, LLC device charges one in every of the capacitances however the energy keep within the capacitor has no likelihood to be transferred to the output,

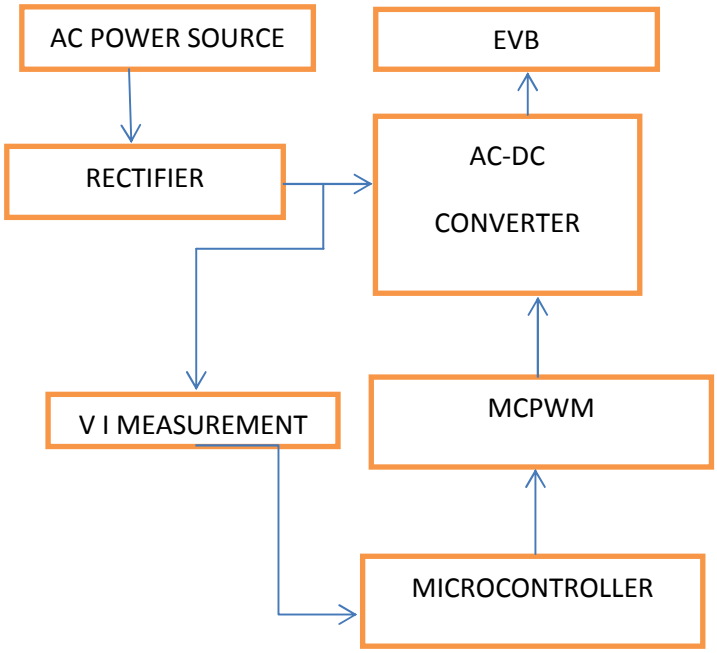
leading to the low utilization iii potency of the auxiliary electrical device. To utilize the auxiliary electrical device totally whereas keeping all the outstanding options of the previous hybrid device. Associate improved hybrid resonant and PWM device is planned in Chapter four. The thought has been verified with simulations.

II.SYSTEM DESIGN

The existing block diagram showed as below,



The proposed system block diagram showed as below



III. SYSTEM SPECIFICATION

A .*Hardware description*

- dc-dc converter
- Step-down transformer
- Current transformer
- Potential transformer
- Microcontroller (ATMEGA8)
- 5V regulated power supply
- Driver circuit
- 12v lead acid battery

B. Software description

- TinyAVR — the AT tiny series
- 0.5–8 kB program memory
- 6–32-pin package
- Limited peripheral set
- MegaAVR — the ATmega series
- 4–256 kB program memory
- 28–100-pin package
- Extended instruction set (Multiply instructions and instructions for handling larger program memories)
- Extensive peripheral set
- XMEGA — the ATmega series
- 16–384 kB program memory
- 44–64–100-pin package (A4, A3, A1)

IV. DESCRIPTION

A. Hardware description

1.dc-dc converter

The basic schematic of a buck–boost device. Completely different topologies area unit referred to as buck–boost device. Each of them will manufacture associate output voltage abundant larger (in absolute magnitude) than the input voltage. Each of them will manufacture a large vary of output voltage from that most output voltage to

nearly zero. The inverting topology – The output voltage is of the other polarity because the input Abuck (step-down) device followed by a lift (step-up) device – The output voltage is of a similar polarity because the input, and might be lower or beyond the input. Such a non-inverting buck-boost device could use one inductance that's used as each the buck inductance and also the boost inductance. The buck–boost device could be a style of DC-to-DC device that has associate output voltage magnitude that's either bigger than or but the input voltage magnitude. it's a switched-mode power provide with an analogous circuit topology to the boost device and also the buck device. The output voltage is adjustable supported the duty cycle of the switch semiconductor unit. One attainable disadvantage of this device is that the switch doesn't have a terminal at ground; this complicates the driving electronic equipment. Also, the polarity of the output voltage is opposite the input voltage. Neither disadvantage is of any consequence if the facility provide is isolated from the load circuit (if, as an example, {the providethe availability|the provision} could be a battery) because the supply and diode polarity will merely be reversed. The switch is on either the bottom facet or the availability facet.

2. Transformer

A electrical device is Associate in Nursing electro-magnetic static device, that transfers power from one circuit to a different, either at constant voltage or at completely different voltage however at constant frequency.

3. Rectifier

The perform of the rectifier is to convert AC to DC current or voltage. Typically within the rectifier circuit full wave bridge rectifier is employed.

4. Filter

The Filter is employed to get rid of the pulsated AC. A filter circuit uses capacitance and electrical device. The perform of the capacitance is to dam the DC voltage and bypass the AC voltage. The perform of the electrical device is to dam the AC voltage and bypass the DC voltage.

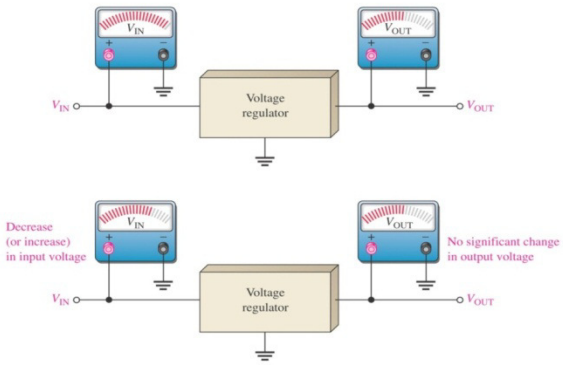
5.Voltage Regulation

•Two basic classes of voltage regulation are:

- line regulation
- load regulation

i. Line Regulation

The purpose of line regulation is to take care of a virtually constant output voltage once the input voltagevaries.The purpose of load regulation is to take care of a virtually constant output voltage once the load varies

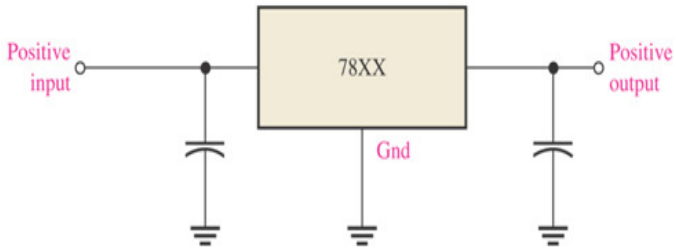


ii. Load regulation

A amendment in load current (due to a variable RL) has much no result on the output voltage of a regulator (within sure limits).Load regulation will be outlined because the share amendment within the output voltage from no-load (NL) to full-load (FL).

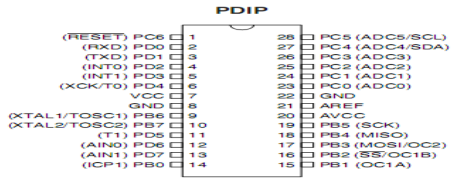
6. Voltage Regulator

The fastened transformer has Associate in nursing unregulated dc input voltage Vi applied to at least one input terminal, a regulated output dc voltage Vo from a second terminal, and therefore the third terminal connected to ground.The series 78XX regulators square measure the three-terminal devices that give a set positive output voltage.



An unregulated input voltage Vi is filtered by a capacitance C1 and connected to the IC's IN terminal. The IC's OUT terminal provides a regulated +12 V, that is filtered by capacitance C2.The third IC terminal is connected to ground (GND).Voltage regulators keep a relentless dc output despite input voltage or load changes. the 2 basic classes of voltage regulators square measure linear and switch. the 2 kinds of linear voltage regulators square measure series and shunt. The 3 kinds of switch square measure change of magnitude, step-down, and inverting.

7. MICROCONTROLLER – ATMEGA 8



i. Port B(PC7.PB0)

Is AN 8-bit bi-directional I/O port with internal pull-up resistors (selected for every bit). The Port B output buffers have symmetrical drive characteristics with each high sink and supply capability. As inputs, Port B pins that ar outwardly force low can supply current if the pull-up resistors ar activated. The Port B pins ar tri-stated once a reset condition becomes active. Even if the clock isn't running.

ii. Port C (PC5..PC0)

Port C is AN 7-bit bi-directional I/O port with internal pull-up resistors (selected for every bit). The Port C output buffers have symmetrical drive characteristics with each high sink and supply capability. As inputs, Port C pins that ar outwardly force low can supply current if the pull-up resistors ar activated. The Port C pins ar tri-stated once a reset condition becomes active, although the clock isn't running.

iii. Port D (PD7..PD0)

Port D is AN 8-bit bi-directional I/O port with internal pull-up resistors (selected for every bit). The Port D output buffers have symmetrical drive characteristics with each high sink and supply capability. As inputs, Port D pins that ar outwardly force low can supply current if the pull-up resistors ar activated. The Port D pins ar tri-stated once a reset condition becomes active, Even if the clock isn't running.

iv. RESET (Reset input)

A low level on this pin for extended than the minimum pulse length can generate a reset, although the clock isn't running. The Shorter pulses don't seem to be sure to generate a reset.

v. AVCC

AVCC is that the offer voltage pin for the A/D device, Port C (3.0), and ADC (7.6). It

ought to be outwardly connected to VCC, although the ADC isn't used. If the ADC is employed, it ought to be connected to VCC through a low-pass filter.

vi. AREF

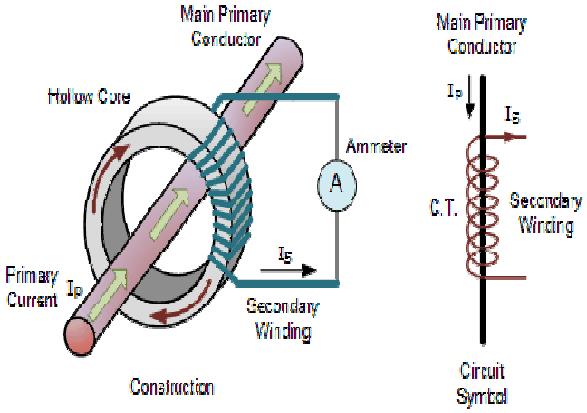
AREF is that the analog reference pin for the A/D device. These pins are battery-powered from the analog offer and function 10-bit ADC channels.

vii. Basic perform

The main perform of the CPU core is to make sure correct program execution. The CPU should so be ready to access reminiscences, perform calculations, management peripherals, and handle interrupts. So as to maximize performance and correspondence, the AVR uses a Harvard design with separate reminiscences and buses for program and knowledge. directions within the Program memory area unit dead with one level pipelining. Whereas one instruction is being dead, following instruction is pre-fetched from the Program memory. This idea allows directions to be dead in each clock cycle. The Program memory is In-System Reprogrammable non-volatile storage. The fast-access Register File contains thirty two x 8-bit general purpose operating registers with one clock cycle interval. This permits single-cycle Arithmetic Logic Unit (ALU) operation. In an exceedingly typical ALU operation, 2 operands area unit output from the Register File, the operation is dead, and therefore the result's keep back within the Register File in one clock cycle. Six of the thirty two registers is used as 3 16-bit indirect address register pointers for knowledge house addressing facultative economical address calculations. one in all the these address pointers may also be used as AN address pointer for research tables in Flash Program memory. These further perform registers area unit the 16-bit X, Y and Z-register. The ALU supports arithmetic and logic operations between registers or between a relentless and a register. Single register operations may also be dead within the ALU. After AN mathematical process, the standing Register is updated to mirror data concerning the results of the operation. The Program flow is provided by conditional and unconditional jump and decision directions, ready to directly address the entire address house. Most AVR directions have one 16-bit word format. Each Program memory address contains a 16- or 32-bit instruction.

viii. Current Transformer *(C.T.)*

Is a style of "instrument transformer" that's designed to supply associate degree electrical energy in its coil that is proportional to the present being measured in its primary. Current transformers scale back high voltage currents to method lower worth and supply a convenient way of safely observance the particular electrical current flowing in associate degree AC cable employing a commonplace meter. The principal of operation of a basic current electrical device is slightly totally different from that of a normal voltage electrical device.



B. Software description

i. AVR32

In 2006 Atmel free microcontrollers supported the new, 32-bit, AVR32 design. They embrace SIMD and DSP directions, together with alternative audio and video process options. This 32-bit family of devices is meant to vie with the ARM based mostly processors. The instruction set is comparable to alternative computer architecture cores, however isn't compatible with the initial AVR or any of the varied ARM cores.

ii. Device design

Flash, EEPROM, and SRAM area unit all integrated onto one chip, removing the necessity for external memory in most applications. Some devices have a parallel external bus choice to permit adding further information memory or memory-mapped devices. the majority devices (except the littlest. TinyAVR chips) have serial interfaces, which might be accustomed connect larger serial EEPROMs or flash chips.

iii. Program memory

Program directions area unit keep in non-volatile flash memory. Though the MCUs area unit 8-bit, every instruction takes one or 2 16-bit words. The size of the program memory is sometimes indicated within the naming of the device itself (e.g., the ATmega64x line has sixty four computer memory unit of flash whereas the ATmega32x line has thirty two kB).There is no provision for off-chip program memory; all code dead by the AVR core should reside within the on-chip flash. However, this limitation doesn't apply to the AT94 FPSLIC AVR/FPGA chips.

C. Internal registers

Atmel ATxmega128A1 in 100-pin TQFPpackage .The AVRs have thirty two single-byte registers and square measure classified as 8-bit computer architecture devices. In most variants of the AVR design, the operating registers square measure mapped in because the initial thirty two memory addresses (000016–001F16) followed by the sixty four I/O registers (002016–005F16).Actual SRAM starts once these register sections (address 006016). Even thorough there square measure separate addressing schemes and optimized opcodes for register file and I/O register access, all will still be self-addressed and manipulated as if they were in SRAM. In the XMEGA variant, the operating register file isn't mapped into the information address space; in and of itself, it's uphill to treat any of the XMEGA's operating registers like they were SRAM. Instead, the I/O registers square measure mapped into the information address area beginning at the terribly starting of the address area. in addition, the quantity of knowledge address area dedicated to I/O registers has mature considerably to 4096 bytes (000016–0FFF16). Like previous generations, however, the quick I/O manipulation directions will solely reach the initial the primary sixty four I/O register locations (the first thirty two locations for bitwise instructions). Following the I/O registers, the XMEGA series sets aside a 4096 computer memory unit vary of the information address area which might be

used optionally for mapping the inner EEPROM to the information address area (100016–1FFF16). The particular SRAM is found once these ranges, beginning at 200016.

i. EEPROM

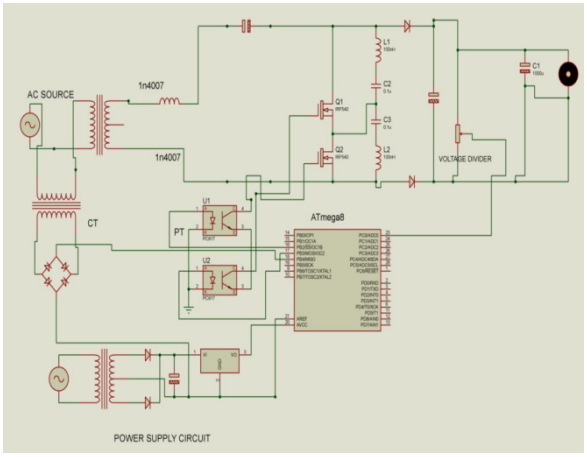
Almost all AVR microcontrollers have internal EEPROM for semi-permanent information storage. Like non-volatile storage, EEPROM will maintain its contents once power is removed. In most variants of the AVR design, this internal EEPROM memory isn't mapped into the MCU's available memory area. It will solely be accessed identical approach Associate in Nursing external electronic equipment is, mistreatment special pointer registers and read/write directions that makes EEPROM access abundant slower than alternative internal RAM. However, some devices within the Secure AVR (AT90SC) family use a special EEPROM mapping to the information or program memory looking on the configuration. The XMEGA family conjointly permits the EEPROM to be mapped into the information address area. Since the amount of rights to EEPROM isn't unlimited- Atmel specifies one hundred,100 write cycles in their datasheets - a elegant EEPROM write routine ought to compare the contents of Associate in Nursing EEPROM address with desired contents Associate in Nursing solely perform an actual write if contents have to be compelled to be modified.

ii. Program execution

Atmel's AVRs have a 2 stage, single level pipeline style. This suggests future machine instruction is fetched because the current one is corporal punishment. Most directions take only 1 or 2 clock cycles, creating AVRs comparatively quick among the eight-bit microcontrollers.

The AVR family of processors were designed with the economical execution of compiledC code in mind and has many

V. CIRCUIT DIAGRAM



VI. HARDWARE SNAPSHOT

VII. CONCLUSION

In this paper, a power management strategy for PV/battery hybrid units in an islanded utility grid has been proposed. The PV/battery unit is control strategy as a

source that employs an adaptive droop control strategy, in contrast to the PV control strategies in the literature where the PV units are controlled to operate as current controlled source (PQ control). It has been shown that controlling the PV/battery unit as a voltage source with the proposed adaptive droop provides the PV/battery hybrid unit with several unique features. First, the hybrid unit has the ability to share the loadpower with other sources while storing any excess energy in the battery. Second, it can track and supply the maximum PV power to the utility grid provided that there is sufficient load demand in the utility grid. Otherwise, the hybrid unit will autonomously match the available load while charging the battery with the excess energy as in standalone strategies. Third, the control strategy modifies the PV operating to follow the load when the total utility grid load is less than the available PV power and battery is fully charged. In addition, the battery may also provide in an islanded utility grid, such as regulating voltage and frequency, and supplying the deficit power in the utility grid.

VIII. REFERENCE

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M.ANANDAKUMAR was completed his under graduation (B.E.,EEE) in the year of 2008 at Sri Subramanya College of Engineering & Technology at Palani and post graduated M.Tech (Power Electronics and Drives) at Karpagam University, Coimbatore in the year of 2011. His teaching experience is more than 7 years and also published more than 5 reputed journals. He is currently working as Assistant Professor in the department of EEE at EXCEL College of Engineering and Technology, Komarapalayam, from August 2016 He has life membership in ISTE, IAENGC . He was also published 03 Engg. College books at Charulatha publication. His research interest involves Renewable energy conversion systems.

R.GUNASEKARAN was completed his under graduation (B.E.,-EEE) in the year of 2003 at Kongu Engineering College, Perundurai and post graduated M.E (Power Electronics & Drives) at KSR College of Technology, Tiruchengode in the year of 2010. He is doing Ph.D.,(part-time) in Anna university, Chennai at 2015 onwards. He is currently working as Assistant professor in the department of EEE at Excel College of Engineering and Technology, komarapalayam from June 2015. His teaching experience is more than 11 years and also published more than 03 reputed journals. He has membership in Indian society for Technical Education (ISTE). He was also published 03 Engg. College books at Charulatha publication. His research interest involves in Power Electronics, Renewable Energy.