RESEARCH ARTICLE OPEN ACCESS

Implementation of Single Phase Cascaded Multilevel Inverter with Multi-Carrier PWM Technique Connected to Grid

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Abstract:

Multilevel inverters are generally used for high power and high voltage applications with reduced amount of harmonic content in its output voltage. Multilevel inverter with increasing number of levels significantly reduces the Total harmonic distortion. The reduced harmonic content in the output voltage is done using multicarrier PWM techniques. A five-level cascaded multilevel inverter with Multi-carrier PWM technique is implemented using MATLAB/SIMULINK. The total harmonic distortion of the output voltage is validated. Also the power flow from the inverter to the grid is validated after incorporating grid integration conditions and it is analyzed with LCL-Filter. A single-phase grid connected Cascaded Multi-level inverter is implemented to feed the grid by setting the reactive power to zero in MATLAB/SIMULINK.

Keywords – **Cascaded H-Bridge, Total Harmonic Distortion, Fast Fourier Transform, Pulse Width Modulation, Modulation Index, PQ Control.**

I.INTRODUCTION

In Recent Years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. The multilevel inverters are mainly controlled with sinusoidal PWM technique and the harmonic contents can be reduced by using various multicarrier PWM techniques[1][4][8]. The multicarrier pulse width modulation cascaded multilevel inverter strategy enhances the fundamental output voltage and reduces total harmonic distortion[2][9]. In addition, there is a need to design filters to reduce the undesirable harmonics in the system[3]. Multilevel inverters are very useful both in grid connected and standalone applications with enhanced capability[5]. In Standalone applications especially in PV generation schemes, the popularity of multilevel inverters has been widely increasing. Cascaded H-bridge multilevel inverter is among the most popular inverter topology in standalone PV systems[6].The need of several sources on the dc side of the converter makes multilevel technology attractive for PV applications. The battery bank for energy storage system is integrated into the topology and hence it can be operating in two modes: battery charging mode and inversion mode. Nowadays the power obtained from solar and wind energy are connected to the grid for better utilization of renewable energy sources. The power extraction from renewable energy sources cannot be directly utilized by the loads or the grid. The power electronic interface such as DC-DC converters and DC-AC inverters especially MLIs are used as an interface between them. The grid can be fed by pure sinusoidal wave or voltage/current with lesser harmonics. To obtain lesser harmonics sinusoidal voltage and current, MLI configuration with LCL filter is incorporated and also the harmonic profile can be improved [7]. DC input voltage sources for the MLI's can be derived from renewable energy sources such as Photo Voltaic array with DC to DC converter [12].

II. MULTILEVEL INVERTER MODELLING USING PULSE GENERATOR

The multilevel inverters have drawn incredible interest in the power industry. They present a new set of features that are well suited for the use in reactive power compensation. Multilevel inverters are more advanced and latest type of power electronic converters that synthesize a desired output voltage from several levels of dc voltages as input. There are three types of multilevel inverters, they are: 1. Diode clamped multilevel inverter. 2. Flying capacitor multilevel inverter. 3.Cascaded multilevel inverter. In this project , Cascaded multilevel inverter is used because it requires less number of components in each level and ((m-1)/2) H-bridges to form the model. Each Separate DC Sources (SDCS) of equal magnitude is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. By different combinations of the four switches, S1-S4, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$, and zero. The output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels is defined by m = 2s+1, where s is the number of dc sources. A five-level cascaded-inverters will have 2 SDCSs and 2 full-bridge cells. The switching table for the five level cascaded inverter is shown below. Here, 2 Full Bridges are used and are cascaded to each other. The Switches S1, S2, S3,and S4 are from upper H-Bridge and Switches S5 S6 S7 and S8 are from lower H-Bridge .By giving correct switching pattern ,we get 5 voltage levels i.e2Vdc,Vdc,0,- 2Vdc,-Vdc.HereV_{dc}=100V each.The most challenging application of this multilevel inverter is interfacing with renewable energy sources.

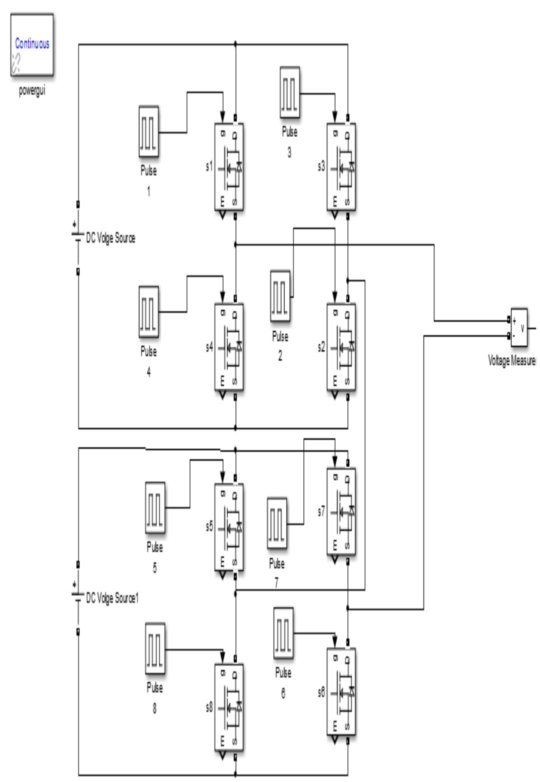

Fig.1. Five-Level Cascaded MLI Using Pulse Generator

Table 1- switching table for 5-level cascaded MLI

OUTPUT	S1	S2	S3	S4	S5	S6	S7	S8
$+V_{dc}$	1	1	0	0	1	0	1	0
$-V_{dc}$	0	0	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0
$+2V_{dc}$	1	1	0	0	1	1	0	0
$-2V_{dc}$	0	0	1	1	0	0	1	1

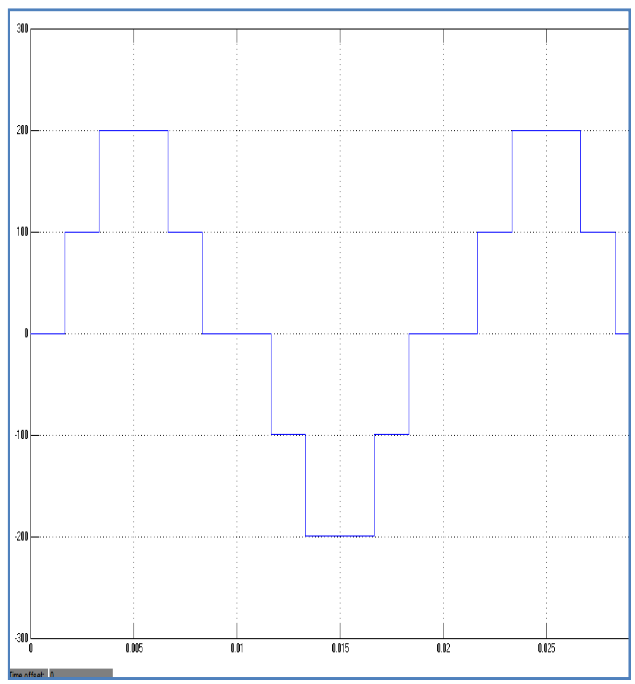

Fig.2. OUTPUT of Five-Level Cascaded MLI Using Pulse Generator

III. 5-LEVEL CASCADED INVERTER MODELLING WITH MULTICARRIER PWM TECHNIQUE

Pulse-width modulation (PWM) of a signal or power source involves the modulation of its duty cycle, to either convey information over a communications channel or control the amount of power sent to a load. There are 3 techniques: **Phase disposition (PD)**- All carrier waveforms are in phase. **Phase opposition disposition (POD)** - All carrier waveforms above zero reference are in phase and are 180 degree out of phase with those below Reference. **Alternate phase disposition (APOD)** - Every carrier waveform is in out of phase with its neighbor carrier by 180. In this modeling we have taken PD PWM technique.

In the model shown below, the DC voltages are of 100V each. The reference and carrier frequency are 50Hz and 5000Hz respectively. The RL type load is connected which is of values R=20Ω and L=47mH which gives 0.8 PF lagging. Here modulation index (MI) can be varied from 0.75 to 1.1 by varying the amplitude of reference(modulating wave) signal.

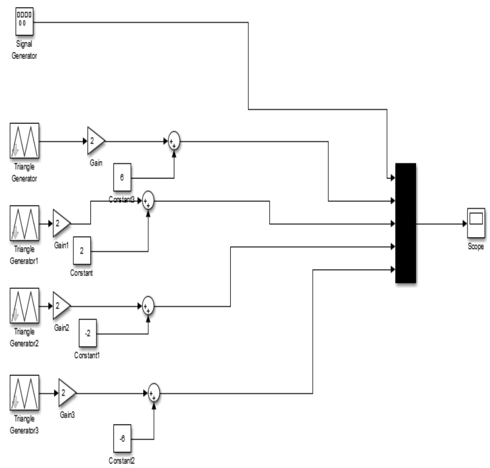

Fig. 3.Simulink model of PD multicarrier gate pulse generation

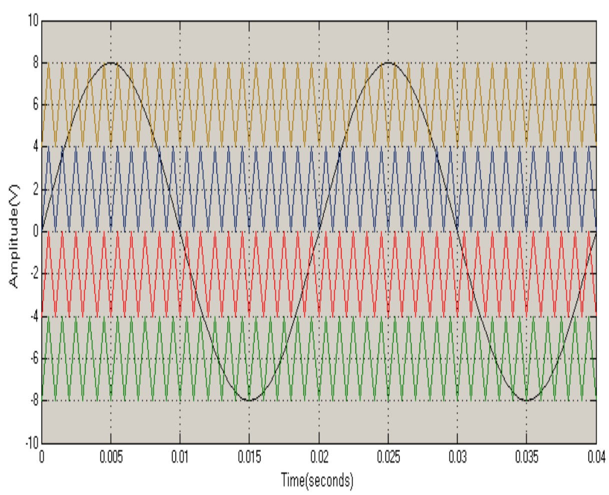

Fig.4. Representation of sine reference and triangular multi-carrier(4)

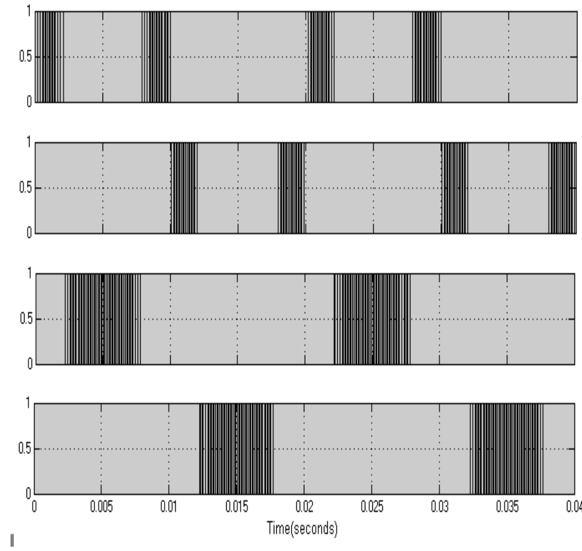

Fig.5. Pulse Generation for 8 switches (with complimentary pairs)

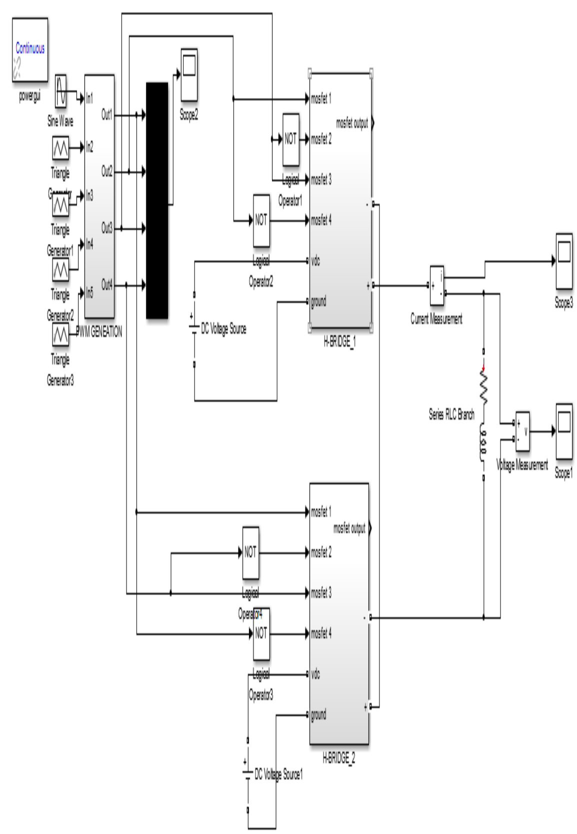

Fig. 6. Simulink Model of the 5-level cascaded inverter with multicarrier PWM

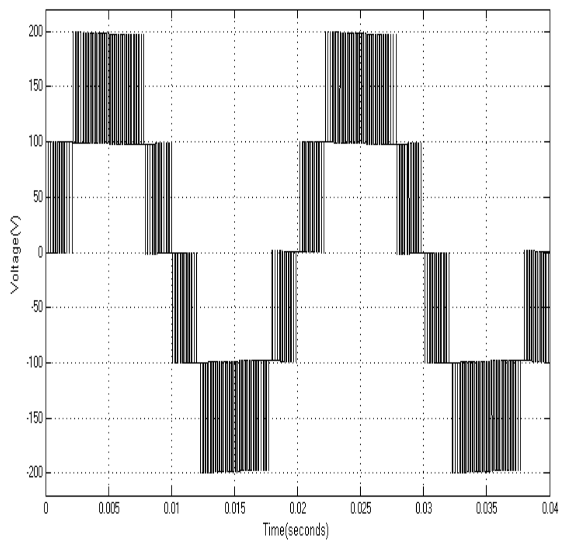

Fig.7. Output Voltage of the 5-level cascaded inverter With MC PWM

IV.TOTAL HARMONIC DISTORTION (THD) ANALYSIS USING FFT WITH FILTERS

The total harmonic distortion (THD) is a performance parameter which describes the quality of a waveform. It can be defined as the measure of closeness in shape between a waveform and its fundamental component. An inverter output consists of fundamental wave which is used to do real work and its harmonics (multiple of fundamental waveform) which causes heat loss in a system. THD is mathematically defined as the ratio of total harmonic content to the fundamental content in a waveform.

$$THD = \frac{\sum_{n=2,3..}^{\infty}(V_{on})^{1/2}}{V_{01}}$$

(1)

where

V_{on} - rms voltage of n th order waveform

n =2,3,4……

V_{01} - rms voltage of fundamental waveform

For an ideal inverter the THD is always 0%. To find the THD, a waveform is expressed in Fourier series as:

$$V_{out} = \frac{a_0}{2} + \sum_{n=1,2,3}^{\infty}(a_n \cos n\omega t + \sin n\omega t) \quad (2)$$

Where,

V_{out}- Fourier series expression of waveform

a_o , a_n, b_n are constants and are defined as,

$$a_0 = \frac{2}{T}\int_0^T V_o(t)dt \quad (3)$$

$$a_n = \frac{2}{T}\int_0^T V_o(t)\cos n\omega t\, dt (4)$$

$$b_n = \frac{2}{T}\int_0^T V_o(t)\sin(n\omega t)\, dt \; (5)$$

Where,

$V_0(t)$ is the output waveform as a periodic function of time.

T is the Time period of the output waveform.

The output filter reduces the harmonics in generated current caused by semiconductor switching. There are several types of filters. The simplest variant is filter inductor connected to the inverter's output. But also combinations with capacitors like LC or LCL can be used. The L-C-L high pass filter produces better attenuation of inverter switching harmonics than the L and L-C filters, So we have used LCL in our design. For Rated power of 1KW,

Table 2 -LCL FILTER DESIGN VALUES

PARAMETERS	VALUE
L_i (inverter side)	8.137mH
L_g(grid side)	4.879mH
C_f Filter capacitance	3μF
R_d (damping Resistor)	10.623Ω

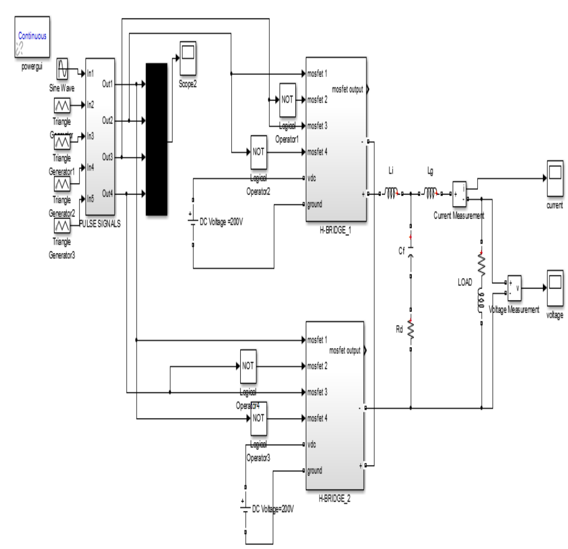

Fig.8. Simulink Model of the 5-level cascaded inverter with LCL-Filter

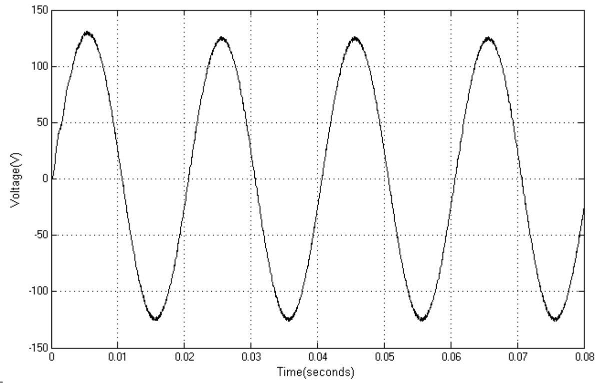

Fig.9. Output Voltage of the 5-level cascaded inverter With LCL-Filter

Fig. 4.16

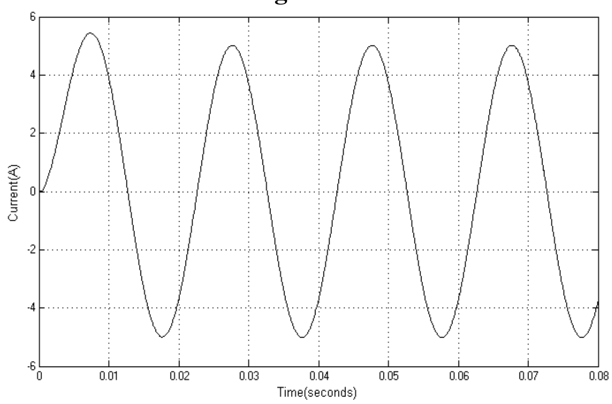

Fig.10. Output Current of the 5-level cascaded inverter With LCL-Filter

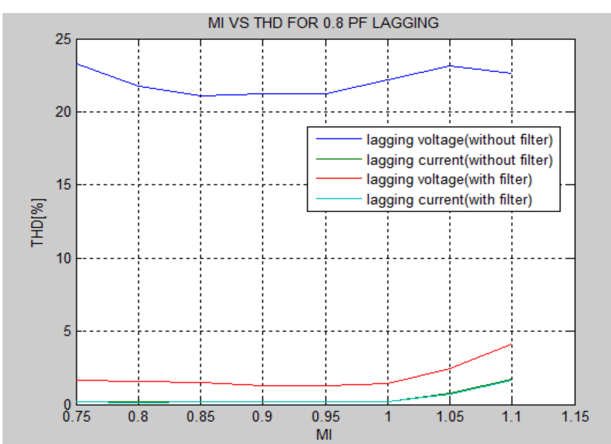

Fig.11. MI VS THD with LCL filter for 0.8 Lagging PF

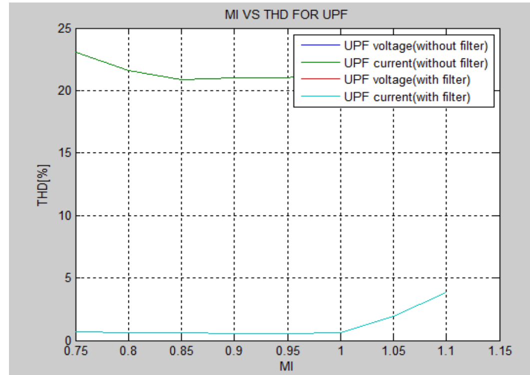

Fig.12.MI VS THD with LCL filter for UPF

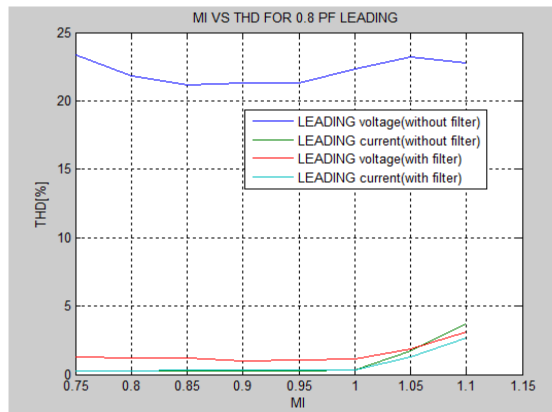

Fig.13.MI VS THD with LCL filter for 0.8 Leading PF

Table 3- THD COMPARISON FOR MI=0.8

LOAD	THD(%) Without filter	THD(%) With filter
R(UPF)	21.60	0.65
RL(LAGGING)	21.78	0.14
RLC(LEADING)	21.85	0.29

V.MODEELING OF GRID CONNECTED CASCADED MLI WITH LCL-FILTER

Grid Integration is done by keeping in view certain constraints. Decoupling inductor is needed to control the power flow from the inverter to the grid, this is provided by the L_g inductor in the LCL filter circuit. V_{inv} has to lead the V_{grid} with certain angle to enable the inverter current to be supplied to the grid.I_{inv} (I_{out}) should be maintained in phase with the V_{grid}. This is achieved by adjusting the phase angle of the modulating wave (reference sine wave).This is done to achieve the Unity power factor operation.(reactive power =0).

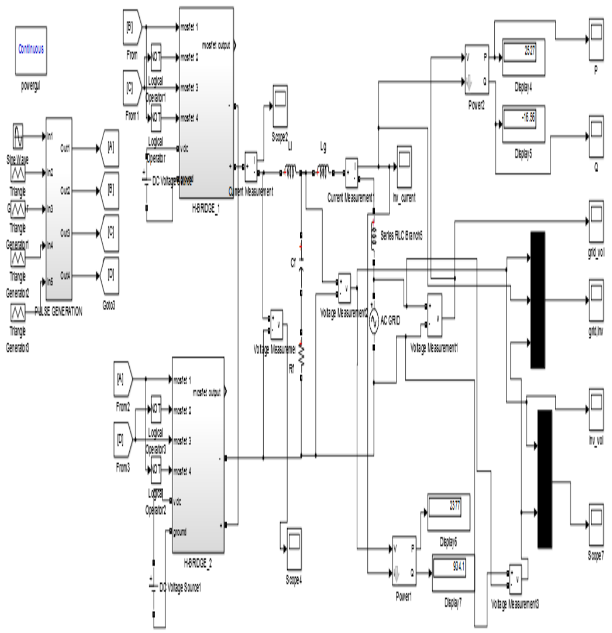

Fig.14. Simulation Model of grid connected cascaded MLI

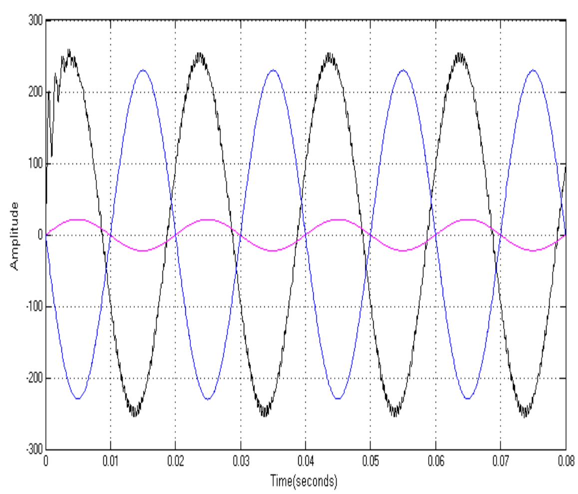

Fig.15. Waveforms of V_{inv}, I_{inv}, V_{grid}

From above, it is observed that V_{inv} leads V_{grid} and V_{grid}, I_{inv} are in phase with each other which is the requirement for the power flow.

By using the PI controller tuning, PQ control is done. The K_p, K_i values are as follows: 0.001, 0.3 respectively. The real power and reactive power are set to 1000 Watts and 0 Watts respectively.

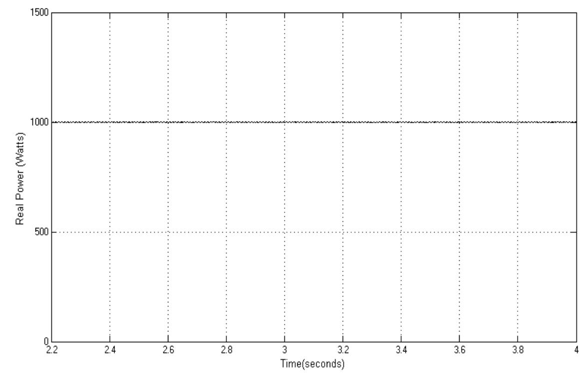

Fig.16. Real power (P = 1000 Watts)

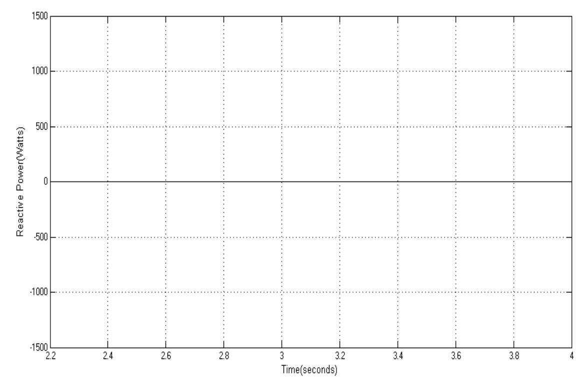

Fig.17. Reactive power (Q = 0 Watts)

VI.CONCLUSION

The cascaded MLI is modeled with Phase disposition (PD) Multi-carrier pulse width modulation technique. The harmonic analysis is done and LCL filter is used to reduce the THD. Finally, Grid is connected to the cascaded MLI with suitable constraints to enable the inverter output current to flow through the grid. Through phase angle adjustment Unity power factor is achieved in the grid such that reactive power Q=0 is maintained. The PQ control is done using the PI controller tuning in the closed loop domain. The present work can be extended to include PV array as a DC source.

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