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Improved Transient Response for Three-Level DC-DCBuck Converter

M. I. Masud[1], S.A. Moiz[1], O Jamil[2*]

[1]Faculty of Electrical Engineering, Umm Al Qura University, Makkah, Kingdom of Saudi Arabia,

[2]Department of Telecommunications, Swinburne University of Technology

Abstract:

Transient response of three level buck converter depends on the slew rate of filter inductance. The slew rate of filter inductor can be increased either by decreasing the inductance magnitude or by increasing the voltage across the inductor. Decreasing the inductance magnitude results in higher losses in the converter due to increase of inductor current ripples. In a three level buck converter, the voltage across the inductor during step up load transient is 0.5Vin-Vout, while during step down load transient is –Vout. For smaller duty cycle applications, three level buck converter offers slow step up and step down load transient response because of limited magnitude of voltage across the inductor. In this paper a new three level buck converter topology is proposed, which will increase the magnitude of voltage across the inductor during load transients and thus will improve the transient response. After load transient, the converter will recover to normal steady state condition and will behave just like a three level converter in steady state. Theoretical and simulation results are presented to show the effectiveness of proposed topology in terms of settling time for step up and step down load transient response.

Keywords-Slew rate, 3-level converter, switching stresses, Settling time, Voltage overshoot and undershoot

I. INTRODUCTION

With the fast market growth of portable applications, demand of high performance power converter increases dramatically [1]. The Dc-Dc Buck converter is one of the most important topology used now days for low power battery operated systems for example PDAs, medical diagnosticequipment's, cellular phones, digital cameras and RF power applications etc [2]. All these applications need high power density, fast transient response, Low switching ripples, low voltage stresses and low switches losses.

In a buck converter with output load current step, the output filter capacitor provides or sinks the immediate difference in current while the inductor current rises or falls linearly to match the new required load current [3-5]. A small inductor allows this change of current rapidly to minimize the output capacitor requirement. However, less magnitude inductor also produces large ripple Several techniques are presented in [7-9], in which slew rate of inductor current is increased by reducing the inductor value during the load transient condition. The reduction in inductance value always results in higher inductor current ripple due to which the higher losses will occurs in the converter.

The step-down load transient is improved in [10]. The derived topology increases the slew rate of inductor current by applying a higher magnitude negative voltage across the inductor. The step down load transient thus improves, but it uses conventional buck converter in steady state which have large switching ripples, large voltage stresses and large filter size.

Another topology for improving dynamic response is presented in [11]. The slew rate of inductor during step down transient response is still limited, as inductor uses the stored energy of flying capacitor which is charged at half of the input

voltage. Therefore, low input voltage increases the step down settling time.

Three level buck converters have four times less inductor current ripple, eight times less output voltage ripple and two times less switching stresses compared to a conventional buck converter [12-13]. It has two times less inductor current ripple, two times less output voltage ripple and two times less voltage stresses comparatively to two phase buck converter [14]. In order to further improve the efficiency of three level buck converters, the transient response should be taken in consideration.

II. PROPOSED TOPOLOGY

Figure.1 shows the proposed 3-level buck converter. This topology has basically 6 Modes of operation. First 4 modes of operation belong to steady state while the mode 5 and mode 6 will be activated only during step down load transient condition and step up load condition respectively, in order to increase the slew rate of inductor current.

A. STEADY STATE OPERATION

The steady State operation of proposed topology is similar to the standard flying capacitor three level buck converter with duty cycle less than 0.5. Figure 2 shows equivalent circuits for different modes of operation.

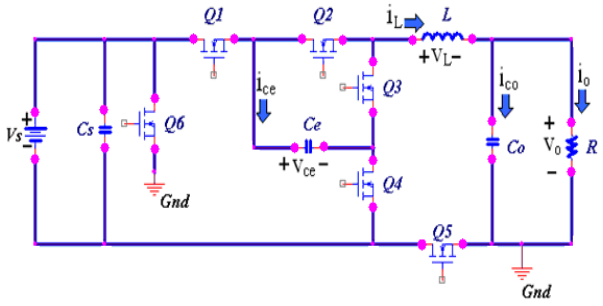


Figure 1. Proposed 3-Level Buck Converter

In mode 1, Switch Q1, Q3 and Q5 will behave as a short circuit and switch Q2, Q4 and Q6 will behave as an open circuit. Capacitor Ce will store energy as it is directly connected to input voltage source. The inductor current in this mode will rise linearly. Similarly, the capacitor Co will store the charges.

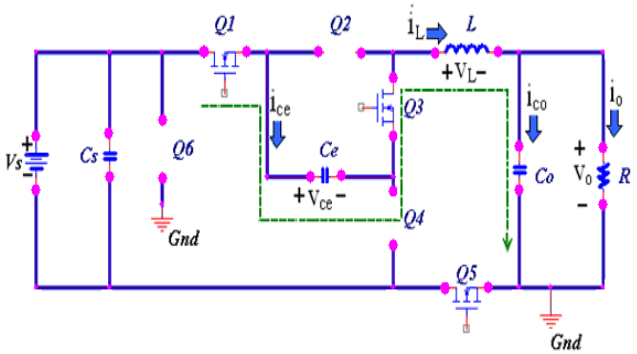
In Mode 2, Switch Q3, Q4 and Q5 will be short circuited and switch Q1 and Q2 and Q6 will be open circuited. The input source will be completely separated from the circuit. The inductor current will fall linearly and the Capacitor Co discharges and its voltage will also decreases. In the meantimecapacitor Ce will also be separated from the load and current through it will be zero, as a result of which the voltage of capacitor Ce will remains constant.

In Mode 3, Switch Q2, Q4 and Q5 will act as a short circuit and switch Q2 and Q4 and Q6 will act as an open circuit. Capacitor Ce will discharge and its voltage will drop slowly. In the mean time the inductor will store energy and current through it will rise linearly. Similarly, the capacitor Co will store the charges. Mode 4 will be similar to mode 2.

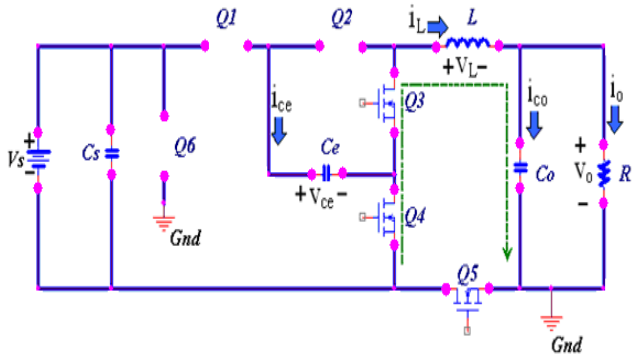
B. TRANSIENT STATE OPERATION

The variation of output load between full load and noload condition generates an overshoot or undershoot in the output voltage. If the load increases than a huge amount of charges will be removed from output capacitor in a very short time interval in order to fulfil the output current demand. This will produce voltage undershoot. Similarly, if the output load decreases than the demand of current will decrease but the current magnitude will not decrease according to the demand in zero time ~~and~~ so excess of current charges will be absorbed by output capacitor as a result of which output voltage overshoots will occurs.

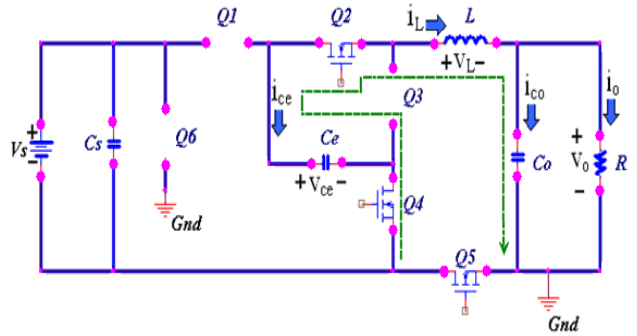
In a 3-level buck converter the inductor current slew rate (rate of change of inductor current) will determine how much the transient response is fast. If the rate of change of inductor current will be fast than the load current will achieve the desired level of current in less time during load transient and hence the overshot or undershoot time duration will be less.



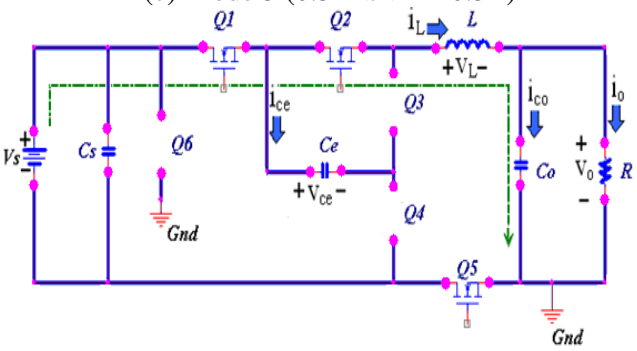
(a) Mode 1 (0<t<DT)



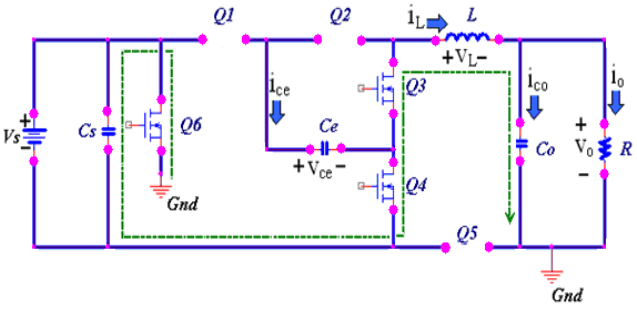
(b) Mode 2 (DT<t<0.5T) and Mode 4 (0.5T+DT<t<T)



(c) Mode 3 (0.5T<t<DT+0.5T)



(e) During step up load transient



(e) during step down load transient

Figure 2. Proposed topology equivalent circuits in different modes (a) Mode 1 (0<t<DT), (b) Mode 2 (DT<t<0.5T) and Mode 4 (0.5T+DT<t<T), (c) Mode 3 (0.5T<t<DT+0.5T), (d) During step up loadtransient, (e) during step down load transient.

For step up transient Switch Q1, Q2 and Q5 will behave as a short circuit and switch Q3, Q4 and Q6 will behave as an open circuit. The equivalent circuit is shown in figure 3(a). The inductor current slew rate will be equal to:

$$\frac{di_L}{dt} = \frac{Vs - Vo}{L} \qquad (1)$$

Where Vs is the input voltage, Vo is the output voltage and L is the inductance.

For the conventional three level buck converter, the inductor current slewrate for step up load transient is given by:

$$\frac{di_L}{dt} = \frac{0.5 * Vs - Vo}{L} \qquad (2)$$

By comparing equation 1 with equation 2 it can be seen that inductor current slew rate for step up transient for the proposed topology is higher than conventional three level buck converter.Thus, proposed converters settling time will be reduced and step up transient response will be improved.

Similarly, for step down transient Switch Q3, Q4 and Q6 will behave as a short circuit and switch Q1, Q2 and Q5 willbehave as an open circuit. The equivalent circuit is shown in figure 3(e). The inductor current slew rate will be equal to:

$$\frac{di_L}{dt} = \frac{-(Vs + Vo)}{L} \qquad (3)$$

For the conventional three level buck converter, the inductor current slew rate for step down load transient is given by:

$$\frac{di_L}{dt} = \frac{-Vo}{L} \qquad (4)$$

By comparing equation 3 with equation 4 it can be seen that inductor current slew rate for step down load transient for the proposed topology is higher than conventional three level buck converter.

This will again improve the step down transient response.

III. THEORETICAL AND SIMULATION RESULTS

In order to verify the effectiveness of proposed 3-level buck converter, the circuit is simulated for following specification: Simulation results are shown in figure 4. For analysing the transient response, first a step down transient is introduced in the circuit at 2.2ms, by load step change of 1 ohm to 2.4371ohm, due to which current changes from 9.8A to 4.1754A. Figure 4(b) shows the simulated results for step down load transient response. The time taken by inductor current from 9.8A to 4.1754A is 6usec in case of proposed

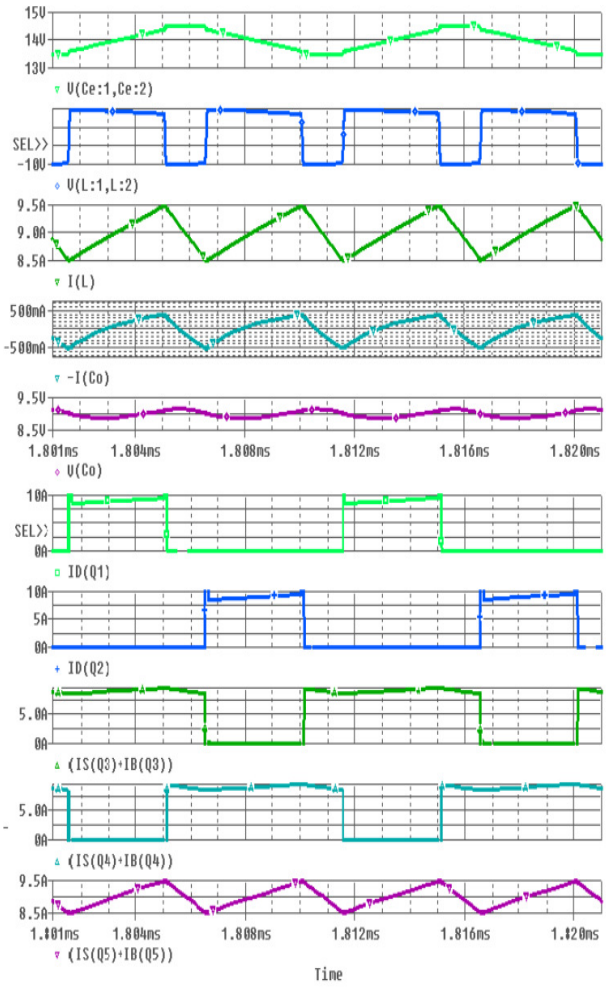


Figure 3(a) Steady state simulation waveforms

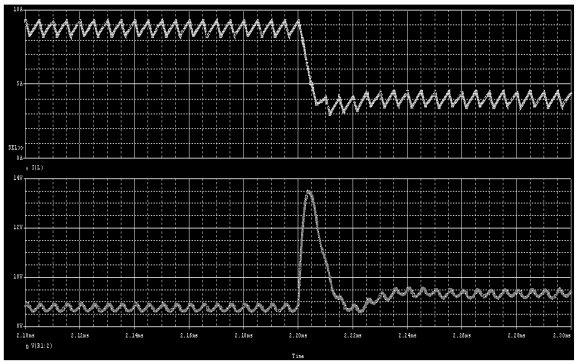


Fig 3(b). Step down transient response current and voltage waveform

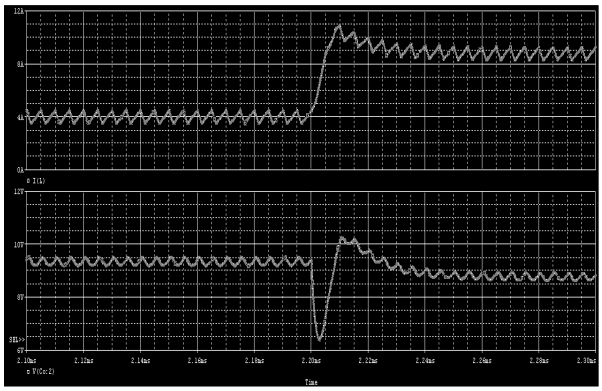


Fig 3(c). Step up transient response current and voltage waveform

Fig 3. Simulation waveforms, (a) Steady state simulation waveforms, (b). Step down transient response current and voltage waveform, (c). Step up transient response current and voltage waveform.

topology and 15.5usec in case of conventional topology. The voltage overshoot is 13.502v in case of propose topology and 16.767v in case of conventional three level buck topology.

To analyse the step up transient response the circuit is simulated again and a load step change of 2.4371 ohm to 1 ohm is introduced this time at 2.2ms, as a result of which the current changes from 4.1754A to 9.8A. Figure 4(c) shows the simulated results for step up load transient response. The time taken by inductor current from 4.1754A to 9.8A is 7.4usec in case of proposed topology and 34.5usec in case of conventional topology. The voltage

undershoot is 6.3842v in case of propose topologyand 5.0955v in case of conventional three level buck topology.

IV. CONCLUSION

The proposed Three level Buck converter topology have fast step up and step down load transient response. The settling time for proposed circuit is much reduced comparatively to conventional three level buck converter. Similarly, the voltage overshoot and voltage undershoot are improved for the proposed topology. The proposed 3-Level buck topology is an attractive and demanding candidate for future low power battery operated portable applications, where converter with fast transient response, low switching ripples, high switching frequency, low filter element size, low switching stresses, low converter size will be the needed

TABLE 1
CIRCUIT SPECIFICATION

Symbol	Parameter Name	Value
Vs	Input voltage	28V
Vo	Output voltage	9.8
Co	Filtering capacitor	2uf
Ce	Flying capacitor	40uf
Cs	Capacitor parallel to supply	40uf
L	Filtering inductance	15uH
f	Switching frequency	100kHz
R	Load step change	1 to 2.4371 ohms

REFERENCES

1. C. Buccella, C. Cecati, H. Latafat, "Digital Control of Power Converters -A Survey", IEEE T Industerial Information, Vol. 8. No. 3, pp. 437-447, 2012.

2. M.H. Taghvaee, M.A.M. Radzi, S.M. Moosavain, H. Hizam, M. H. Marhaban, "A current and future study on non-isolated DC–DC converters for photovoltaic applications", Renewable and Sustainable Energy Reviews, Vol. 17, pp. 216–227, 2013

3. H. Komurcugil, "Non-singular terminal sliding-mode control of DC–DC buck converters", Control Engineering Practice, Vol. 21 , No.3 , pp. 321-332 , 2013.

4. Tan, S.-C., Lai, Y.M., Cheung, M.K.H., Tse, C.K., **"**On the practical design of a sliding mode voltage controlled buck converter**",***IEEE Transactions on Power Electronics,* Vol.20, No. 2 , pp. 425-437, 2005.

5. Y. Zhang, X. T. Sun, Y. F. Wang, H J. Shao, "Transformerless three-level DC-DC buck converter with a high step-down conversion ratio" *Journal of Power Electronics,* Vol.13, No. 1 , pp. 70-76, 2013.

6. M. El-Zanaty, M. Orabi, M. Z. El-Sadek "Review of Synchronous Buck Converter Design Optimization" MEPCON 2008, 12th International Middle-East Power System Conference, pp. 588 – 592, 12-12 March 2008.

7. N. K. Poon, C. P. Liu, and M. H. Pong, "A low cost dc-dc stepping inductance voltage regulator with fast transient loading response," in Proc. Appl. Power Electron. Conf. Exp. (APEC 2001), Anaheim, CA, vol. 1, pp. 268–272, 2001.

8. K. Yao, Y. Qiu, M. Xu and F. C. Lee, "A novel winding-coupled buck converter for high-frequency, high step-down DC-DC conversion." IEEE transactions on power electronics, Vol.20, No.5, pp.651-656, 2005.

9. S. A. Wibowo, Z. Ting, M. Kono and H. Kobayashi "Analysis of coupled inductors for low ripple fast-response buck converter." IEEE Asia Pacific Conference on Circuits and Systems, 2008. APCCAS 2008. pp. 1860-1863, 2008.

10. R. Pal Singh, A. M. Khambadkone"A Buck-Derived Topology with Improved Step-Down Transient Performance" IEEE T.Power Electronics, Vol. 23, No. 6, pp. 2855-2866, 2008.

11. L. Shi, M. Ferdowsi, M. Crow, "Dynamic response improvement in a three-level buck type converter," *IEEE 2010 Energy Conversion Congress and Exposition*, 2010, pp.1952-1958.

12. V. Yousefzadeh, E. Alarcón, D. Maksimovic "Three-Level Buck Converter for Envelope Tracking Applications" IEEE T.Power Electronics, Vol. 21, No. 2, pp. 549-552, 2006

13. X. Ruan, B. Li, Q. Chen, S.-C. Tan and C. K. Tse, "Fundamental considerations of three-level dc–dc converters: topologies, analyses, and control," IEEE transactions on circuit and systems, Vol. 55, No.11, pp. 3733-3743, 2008.

14. D. Garinto, "A new converter architecture for future generations of microprocessors." CES/IEEE 5th International Power Electronics and Motion Control Conference, 2006. IPEMC 2006., pp. 1-5, 2006.