A SURVEY ON 10-BIT PIPELINE ADC SUITABLE FOR VIDEO APPLICATIONS

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ABSTRACT

A 10 bit low voltage low power pipelined ADCsuitable for a video application ispresented. The presented architecture utilizes a combination of parallel sampling technique and op-amp sharing technique. The architecture consists of several blocks such as amplifier,MUX,flashADC, reconstructionblock,T/H (Track and hold Amplifier) etc.T/His essential for multistage ADCs.Multiplexer is used to select any one of the parallel paths in parallel sampling technique.Reconstruction block helps to avoid excessive clipping noise and achieving good linearity.A flash ADC is a type of ADC that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages. To achieve low power, a folded cascade OTA and low power dynamic comparator is used. In this design 10 bit pipelined ADCconsumes a total power of 18.0279mW.This design is implemented in 180nm technology using cadence software.

KEYWORDS: low power, parallel sampling MDAC, pipelinedADC, op-amp sharing MDAC, video applications.

I. INTRODUCTION

Analog to Digital converters are the most important building blocks in lots of applications. As electronics and telecommunication worlds are moving fast towards digitalization and there is an ever increasing demand on speed and accuracy of the processed data, the need for high speed and high resolution ADCs has grown dramatically over recent years. There are many types of ADCs that one can choose between them, but based on the application specification and the requirements on speed, resolution, power and area the most suitable architecture can be chosen.

An ADC is defined by its bandwidth (the range of frequencies it can measure) and its signal to noise ratio (how accurately it can measure a signal relative to the noise it introduces). The resolution of the converter indicates the number of discrete values it can produce over the range of analog values. The values are usually stored electronically in binary form, so resolution is usually expressed in bits. A direct-conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, capable of gigahertz sampling rates. But this type of ADC's have a large die size, a high input capacitance, high power dissipation, and are prone to produce glitches at the output. They are often used for video, wideband communications or other fast signals in optical storage.

A successive approximation ADC uses a comparator to successively narrow a range that contains the input

voltage. At each successive step, the converter compares the input voltage to the output of an internal digital to analog converter which might represent the midpoint of a selected voltage range. At each step in this process, a sigma-delta ADC (also known as a delta-sigma ADC) oversamples the desired signal by a large factor and filters the desired signal band. Generally, a smaller number of bits than required are converted using a Flash ADC after the filter. The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies. A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output approximation is stored in a successive approximation register (SAR). The steps are continued until the desired resolution is reached.

II.PIPELINED ADC

Target applications for pipeline ADCs [31]include communication systems, in which total harmonic distortion(THD), spurious-free dynamic range (SFDR), and other frequency-domain specifications are significant; CCD-based imaging systems, in which favorable time-domain specifications for noise, bandwidth, and fast transient response guarantee quick settling; and data-acquisition systems, in which time and frequency domain characteristics are both important. Fast and accurate N-bit conversions can be accomplished using at least two or more steps of pipelining.

III.Study of various existingtechniques on video applications

With the rapidly growing demand of high-speed signal processing applications such as HDTV's, digital camcorders, medical imaging equipment's, and portable data communications, the analog-to-digital converters(ADC's) for the systems need the characteristics of alow-supply voltage, a low-power consumption, a lob-level resolution, and a more than 40 Msample/s data sampling rate [18]-[20]. Traditionally the ADC's have been implemented in BJT or BiCMOS technologies due to high-speed targets. However, the ADC's have drawbacks in a large power dissipation, a large chip area, and incompatibility with CMOS on-chip digital circuits [21]-[22]. The ADC's based on the CMOS technologies could solve the problems partially, but the required tight specificatons on power, speed, and resolution were difficult to be met simultaneously [20], [23]-[24]. Moreover, variable on-board supply voltages from 3V to **5V** need to be considered for wide system applications of the ADC's. Hence based on existing techniques on video applications power consumption is high and has bottlenecks of sharing voltages which in turns have circuit complexity, reduced speed with large area. In order to achieve high speed with reduced system complexity, low power and reduced die area a proposed technique of parallel sampling, op-amp sharing is proposed.

3.1 Analog to digital conversion for video applications using cmos technology

A low power dissipation in analog to digital converter for video application is achieved by means of 3.3v OTA, dynamiccomparator, pipeline scaling using cmos technology. However it has the bottle neck i.e. scaling also requires tighter capacitor matching in first stages of pipeline, which in turn increases system

complexity with addition of capacitors and a smaller sampling capacitance can be chosen for high speed or low power but it is likely to result in non-manufacturable design due to capacitor matching accuracy.

3.2 Channel length adjustment technique

The short channel effect observed frequently in deep submicron cmos technologies. The drain current of a transistor is used as a current mirror is changed much by drain source voltage variations of the transistor. The secondary effect resulting from supply voltage variations and transient noise during circuit operations degrade the performance of analog core circuit such as op-amp and increases power consumption of the system. In order to overcome the above problem a channel length adjustment technique is proposed with an addition of two transistors to a conventional bias circuit and by selectively adjusting the channel length of the transistor in bias circuit. It has the advantage of minimizing the mismatch between bias currents due to channel effect by supply voltage variations. The drawback of above technique it has no guarantee of above two extra transistors will operate in saturation region.

3.3 Gate bootstrapping technique

Boot strapping [36]circuits could reduce signal distortion by keeping the gate source voltage of sampling switches constant independently of input signal levels. In high frequency applications the signal current may have large amplitude that it produces [37] a significant voltage drop in bottom sampling switch on resistance. The drawback of above technique is, due to bottom sampling switch is connected between the input of the amplifier and the charge escaping from the boot strapping circuit may distort the sampled signal charge.

3.4 Biasing technique for a gain boosting telescopic amplifier

It is widely used for high open loop gain and excellent bandwidth with less power consumption. One undesirable characteristics of telescopic amplifier is that they typically have a relatively small input common mode voltage and output swing range due to too many transistors cascade together. The operation of transistor to be in saturation region depends upon process and temperature. Hence more critical to use in low voltage applications and has the total power consumption of 60mW.

3.5 Skew insensitive double sampling

Double sampling technique increases the sampling rate with only a minor increase in power. Due to parallelism circuit needed for implementation the above double sampling technique suffers with a problem of timing skew. In order to avoid the above drawback an additional switch is needed to act as mux and also has the power consumption of 135mW.

3.6 Pipeline architecture and time interleaved architecture

There are many schemes used in the pipeline architecture to reduce the power consumption of the ADC. However, the pseudo differential architecture could not provide a good dynamic performance for the relatively high frequency inputs due to its non-differential nature and hence the higher even order harmonics compared with that of the fully differential one. Also, the time-interleaving architecture could not show a good dynamic performance due to the mismatches between the time-interleaving

channels and usually needs complex calibration scheme to correct the mismatches .

3.7 An architectural partitioning optimization analysis

An architectural partitioning optimization analysis [38]-[41] of the classical pipeline ADC has been carried out for high-bandwidth and low-power mobile video applications. It is found that2.5-bit inter-stage resolution is optimal for 10-bit

SL.NO.	PIPELINED ADC	APPLICATION	TECHNOLOGY	POWER	RESOLUTION	MSPS	Power supply	area	Input frequency	FOM,ENOB	SNR/SFDR/SNDR	DNL/INL
1.	(1)	Wimax transceiver	Bicmos 0.35um		12	40Ms/s					28 SFDR	
2.	(2)	Video- digital video broadcasting over cable (DVB-C), terrestrial (DVB-T) and handheld (DVB-H)	0.25-μm CMOS	60 mW	10	30MSPS	3	1.36 mm^2.	60MHz	9.09 bits	SNDR-56.51 dB SNR-56.78 dB SFDR-71.94 dB	0.4 (LSB) /0.85 LSB
3.	[4]	Video	12	23mW		20MS/S	2.6-3.3	1.1mm^2	4:4995 MHz		SNR-63.1 dB SFDR -66 dB	
4.	[5]	Video	0.8 um CMOS	119 mW/ 320 mW	10		3/5		40MHz/50 MHz			
5.	[6]	High Frame-Rate Video/Image Capturing Instruments and Systems	0.25 µm 1P5M CMOS			80	3.0 V	1.99 ×1.65 mm^2	12.734MHz	9.39 bits	SNDR-58.29 Db	
6.	[7]	video ADCs for mobile/handheld receivers	0.35- m CMOS	19.5mW	10	20.48 MS/s	1.5	1.3mm^2	100-MHz	0.19 pJ,9.01 bits	56-dB SNR,SFDR-60dB	-0.1 to+0.3 LSB/-3.4 to +2.7LSB
7.	[8]	Video-HDTV	90nm	56mW		165	1.2	0.15 mm^2			SNR-55dB	
8.	[10]	Wireless- baseband transceiver	0.25µmCMOS	311mW	13 bit/Dual 12 bit	180	2.7		400MHZ	10.6 bits@ 15 MHZ/9.7 @100MHz	SFDR-62 dB	0.28/ 0.38 LSB and the INL is 0.48/ 0.44 LSB
9.	[11]	WiMAX	0.13-µm CMOS process	55mW	12	50	2.5		50MHz	11.3 bits	SFDR-76mW,SNDR-69mW	
10	[12]	Wireless-Multi-Channel Wireless LAN		1.2 W	2	180	3.3		2.4 ghz		SNR-61 dB	
11	[13]	WIRELESS RECIVER	CMOS 0.18um	32Mw	10	50	1.8	1.4 mm^2	2ghz	10 bit	SNDR- 61 dB,SFDR -73dB	±0.5 LSB/+-.55 LSB
12	[14]	Wireless-Wireless LAN	0.25- m	12mW	10	40	2.5			9.3 bit	SNR-61.3dB@ 10.6MHz SNDR-	0.77LSB/ 1.15LSB

											57.6dB@ 1 MHz,57.8 dB@19.3 MHz	

Table1: PIPELINED ADC

PipelineADCresolutions irrespective of sampling rate. But it has the drawback input and output swing limitations and amplifier settling accuracy for subsampling applications, the power consumption is 19.5mW.

3.8 Double sampling

Each stage in the circuit uses the above technique along with its own op-amp. Each stage has two capacitors which sample the input frequency [35] $f_s/2$ but the sampling frequency of whole ADC is f_s. Hence it increase the speed of ADC with reduced power but this technique doubles the no. of capacitors thus op-amp is active in both phases, there is a potential problem of introducing a correlation between consecutive samples. Due to the finite gain of the op-amp, a charge is injected in the input parasitic capacitance which never resets. Therefore, the output voltage will be a recursive function of the present and the previous samples causes memory effect problem [25]

3.9 Dynamic memory effect cancellation technique

The above technique is widely proposed to reduce the memory effect problem which is stated in previous technique. The technique can be sorted into three categories. First, an additional clock phase is employed to reset the op-amp input [26]. Even if resetting the residual charge at the input of the op-amp can eliminate the memory effect, this approach Increases the bandwidth requirement of op-amps since the settling time is reduced due to the additional reset phase. Second, a dual input pair, which operates in alternative clock phase, is employed in the op-amp [26], [27]. While one input pair is used as the input of an op-amp, the other unused pair is reset to common bias voltage to discharge the residual charge related to the output of the previous phase. Since those two input pairs have different characteristics, this technique is suitable for op-amp sharing between two adjacent stages in a single channel ADC. Third, background digital self-calibration can be used in ADCs [28]. However, the implementation of Calibration tends to become complex and occupy more silicon area.

IV Proposed technique on video application

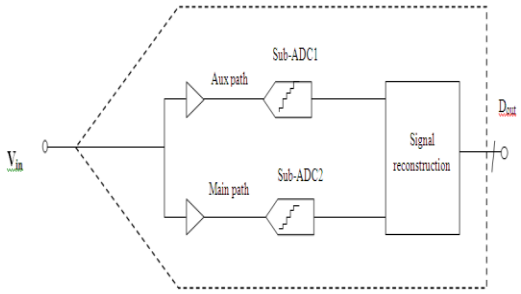
4.1 Parallel sampling technique

In parallel sampling technique [29] the ADC consists oftwo parallel sub ADCs, each of them preceded by a range scaling stage and their outputs are combined by a signal reconstruction block. The block diagram an ADC with parallel sampling technique is shown in figure 1. The front end input signal is split into two signals which are just scaled versions of each other after the range scaling stages. The signal in the main path has the same strength as the front end input signal, while the signal in the auxiliary path is an attenuated version of the front end input signal. These two signals are sampled by the sub ADC at the same time. [42]- [48].

Depending on the input signal level, one of them will be chosen to reconstruct the signal in the digital domain. Since the sub

ADC in the auxiliary path quantizes an attenuated version of the ADC input signal which has lower probability of saturating the sub ADC and a better linearity. During amplitude samples of the main path, hence avoiding excessive clipping noise and achieving good overall linearity

FIG.1Block diagram of an ADC with the parallel sampling technique



The pipelined ADC with parallel sampling technique is shown in figure1. It consists of a number of cascaded stages. The first stage of the proposed pipeline ADC is implemented with parallel sampling technique is the most critical one in terms of speed and noise performance, hence consuming significant power.

In this ADC, the first stage is not preceded by a dedicated sample and hold amplifier; this reduces further the total power consumption. There are three paths for the input signals main signal path, auxiliary signal path and detection path. The main and auxiliary signal path each consists of a signal scaling block anda passive sampling network (T/H) and they are multiplexed by a channel selection block (MUX) to a subtraction block and then to the amplification block (AMP). The detection path consists of a flash ADC and a DAC.

signal reconstruction, the auxiliary path provides coarsely quantized samples to replace the clipped or highly distorted large

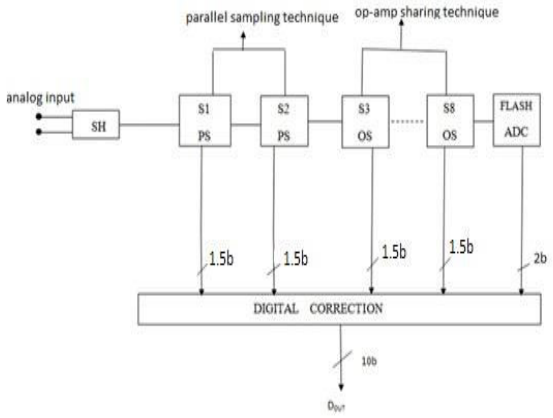
4.2OP-AMP SHARING TECHNIQUE

Significant power saving can be achieved if one operational amplifier is shared between two consecutive stages of the pipelined converter, as shown in figure 3.3. In op-amp sharing technique an op-amp is shared between two successive stages in a pipelined ADC. The main advantage of using op-amp sharing technique is that, the number of amplifiers is halved compared to the basic pipelined ADC architecture. However, the total power dissipation is reduced by one third.

4.3 Hybrid architecture using parallel sampling and op-amp sharing

The front end sample and hold (SH) and the first 2 stages (S1, S2) uses parallel sampling technique [30]. Sample and hold amplifier is added to sample the input and hold the signal information at the sampled value during the time in which the conversion into a digital number is performed. The stages S3 to S8 use op-amp sharing technique. This architecture combines the advantages of parallel sampling technique and op-amp sharing technique and attenuates their drawbacks. This architecture reduces the power consumption in pipelined ADC.

Fig.2 Block diagram of parallel sampling and op-amp sharing technique



In parallel sampling technique the ADC consists of two parallel sub ADCs , each of them preceded by a range scaling stage and their outputs are combined by a signal reconstruction block. . The front end input signal is split into two signals which are just scaled versions of each other after the range scaling stages. The signal in the main path has the same strength as the front end input signal, while the signal in the auxiliary path is an attenuated version of the front end input signal. These two signals are sampled by the sub ADC at the same time. Depending on the input signal level, one of them will be chosen to reconstruct the signal in the digital domain. In an op-amp sharing technique, an op-amp is shared between two successive stages of a pipelined ADC. This stage consists of a folded cascode OTA [32] and op-amp sharing MDAC and sub ADCs and sub DACs. Limited input output voltage swing is the main drawback of telescopicoperational amplifier. In order to alleviate the drawbacks of telescopic op-amps, a folded cascode operational transconductance amplifier can be used. Folded cascode OTA is [33] basically an op-amp without an output buffer and can only drive capacitive loads. The overall voltage swing of a folded cascode OTA is only slightly higher than that of a telescopic configuration. The primary advantage of the folded structure lies in the choice of the voltage levels because it does not stack the cascode transistor on the top of the input device. Folded cascode OTA is used for high speed and dynamic range applications.

v.Conclusion

The proposed architecture consists of 9 stages .The first two stages uses parallel sampling technique and next six stages use op-amp sharing technique. The last stage is a 2bit flash ADC,parallel sampling stage consists of several blocks such as parallel sampling MDAC,flashADC, a DAC unit,amplifier and a comparator circuit.Aparallel sampling MDAC consists of multiplexer circuit and an amplifier circuit.An op-amp sharing consists of an op-amp sharing MDACand two sub ADCs and two sub DACs.A folded cascade OTA is chosen for this application because of its low power consumption and improved output voltage swing.

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