A Pipelined ADC With Sub-ADC Based on Flash–Ramp Architecture

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Abstract— *This work is base on the pipeline ADCs architecture. Pipeline ADCs are convenient alternatives to time interleaving. As the stage of the pipeline is simpler asd compare to a full converter, the design area and power are competitive. The pipeline ADC design with two or more stages in which every stage is of a low resolution ADC, and combining these stages results in a higher resolution.The design ADC consists of channels for high operating speed and every channel consist of a pipelined flash and ramp analog 5to digital converter architecture with reduce power and a optimize area. The sample ADC design in a 50-nanometer CMOS technology with 8-bit of resolution. The supply voltage is 1.2V.*

Keywords:Flash ADC, Ramp ADC, Pipelined, SAR, Dual Slop

Introduction:

In wireless communication a high resolution asnd high speed in the raange of GS/s analog to digital data converter is required.The speed of ADCs are depends on the internal clock.The conversion time of SAR converter for N bit will be N clock cycle. It is for Ramp converter is 2^N-1 clock cycle for N bit conversion. The speed of ADC is affected due to their short sampling period. Resolution is define as the smallest change in the analog input will the change in the digital. It is also related to the step size, since it is the amount that output voltage will change as the digital input value is change from one step to the next.

The power dissipation increases with the sampling in the range og GS/s. The Successive Approximation Register ADC is a single channel simple structure architecture allows high spped conversion with reduces power dissipation. To improve the sampling rate limit a time interleaved ADC with theFor the N channel bandwidth the time interleaved structure is N times the one of the single channel used. Such an approach is restricted by the fact that integrating a huge number of channels increases the complication of the clock distribution and causesthe sampling errors.

Pipeline Analog To Digital Converter:

The pipeline ADC design with two or more stages in which each stage is of a low resolution ADC, and combining these stages results in a higher resolution. Each stage requiring an around equal span of time to perform. The stages are then ordered into a chain. The first stage executes a coarse conversion. In a succeeding step, the variation to the input signal is defined using a sub digital to analog converter. This variation is passed on to the following stages and the process is againg continued with repeatetion before digitally combining the outputs of all of the stages to finish the conversion. When first stage completes first step of operation of the sequence, then stage1 passes the processed data or sample to the stage2whichcompleted the step2 operation of the pipelined process and the data is passes to its next stages. Thus, the next stages can be processedparallely, and this enhances the data conversion rate, or in the case of signal processing systems, enhances the conversion rate at which data are processed [1].

The latency i.e number of samples per unit time of converter is the same as to the number of stages in the pipeline architecture multiplied by the time required to perform the slowest stage. This kind of Analog to Digital Converter is high-speed, has a high resolution with optimize area as compare with the Flash type Analog to Digital Converter.

Every stages of pipeline architecture (Fig 1) Analog to Digital Converter comprises of a sample & Hold circuit to sampled analog voltage to be converted and hold the sampled data, an N-bit flash

ADC for high speed operation, a reconstruction DAC, a subtractor, and a residue amplifier [1].

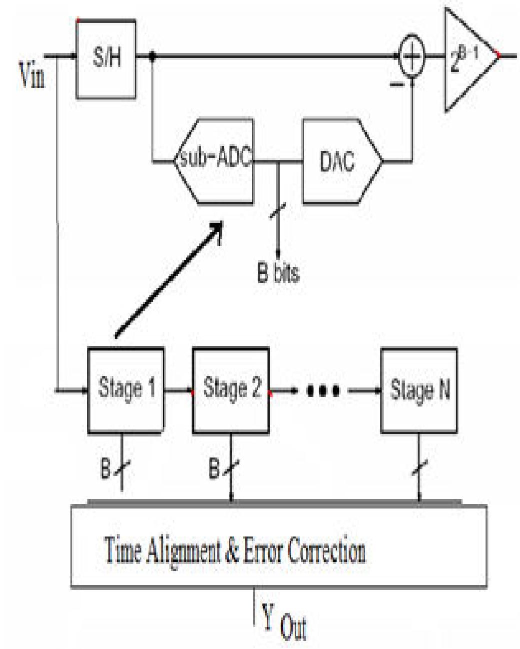

Fig 1: Pipelined ADC [1]

The conversion process startsallowing the sample-and-hold circuit operates in the hold mode followed by a stage1 analog to digital converter conversionfor the most significant bits (MSB).. The converted (processed) digital data of the MSB converter drives the stage2 analog to digital converter which makes a coarsely quantized version of the analog input signal. The stage1 bit ofdigital to analog converter output is subtracted from the hold analog signal, amplified, and applied to the stage2 bit least significant bit ADC.

Successive Approximation ADC:

With the technology scaling, successive approximation register (SAR Fig 2) ADCs are broadly used. This is due toits high power efficiency and optimized area [2]. SAR uses registerinstead of counters. It works as:

1. 1. The analog voltage which is to be converted is at Va input. Let it be 10.45, The output node of all registers are reset to zero so that the output is as Q=0000. This digital putput is fed to the input termainal of DAC which convert it in analog voltage form as shows at time t0 on the timing diagram. At comparator VAx<VA,so its output is at logic '1'.
2. The control logic set or reset the node of register, initially it set the output node of first register to logic '1' level at the time t1. This makes the output of register as "1000". This output is converted at voltage equivalent level of 8V by DAC and with the comparison of VAx and 8V. the comparator output is still high. This high shows that the setting first register not make VAx exceed VA so that control logic keep this level.
3. Atthe time t2 on timing diagram shown in fig , control logic sets the second registre at logic'1', this makes the register output as Q="1100". This output is again converted at voltage level of 12V. Now the output of DAC makes the VAx voltage less than VA and the comparator output output level goes to "0". The logic low level at comparator output node shows that the analog voltage at VAx is larger. This makes control logic to reset the second bit of register at time t3. Now the content of register is Q="1000" and DAC output back to 8V.
4. The control logic sets the third bit of the register and it makes the register output as Q="1010". This output is again converted at voltage level of 10V. Now the output of DAC makes the VAx voltage larger than VA and the comparator output output level goes to "1". The logic high level at comparator output node shows that the analog voltage at VAx is less. This makes control logic to keep its third bit of register.
5. At thelast step at time t5 on timing diagram, control logic sets the fourth registre at logic'1', this makes the register output as Q="1011". This output is again converted at voltage level of 11V. Now the output of DAC makes the VAx voltage greater than VA and the comparator output output level goes to "0". The logic low level at comparator output node shows that the analog voltage at VAx is larger. This makes control logic to reset the fourth bit of register at time t5.

Now the content of register is Q="1010" and DAC output back to 10V.

At time t6 control logic operates on all the four register bits and the conversion process is finished and the control logic activates end of conversion (EOC) command. The converted digital data equivalent to analog voltage is in the register. This converted data is quite which is less than the actual analog input voltage, that's why it is called as successive approximation ADC. In this conversion the control logic goes to each register bit, set it to 1and goes on to the next bit. The processing of each bit take one clock cycle, so that the total conversion time for N bit converter will be equal to N clock cycles.

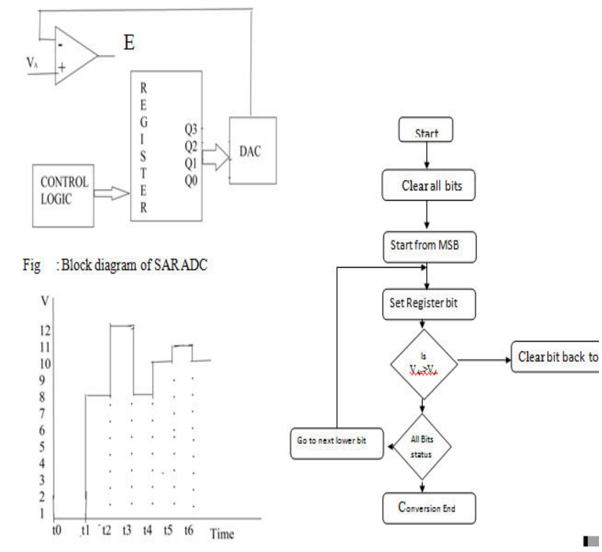

Fig 2: Block Diagram and operating flow of SAR ADC

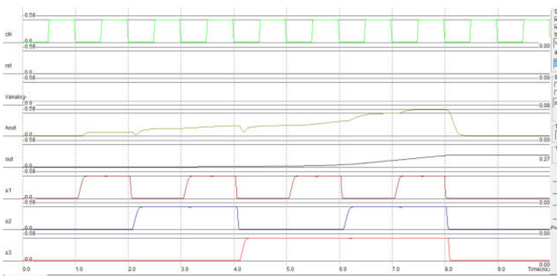

Fig 3: Timing Simulation of SAR ADC

I. Flash ADC:

The flash ADC (Fig 3) is the fastest ADC with more hardware as compare to other ADCs. The N bit ADC requires 2^n-1 analog comparator and 2^n resistor. For 3 bit ADC, 7 comparator and 8 resistor required. The voltage divider setup reference level for each comparator so that there are seven levels corresponding to 1V (weight of LSB), 2V, 3V,…. The analog input Va is connected to other input of each comparator. With Va<1V, all the comparator output C1 to C7 will be high. With Va>1V, one or more than one comparator will be LOW. The comparator output are fed to one active low priority encoder that generates a binary output corresponding to the highest number comparator output that is low. For example when Va is between 3 & 4 volt, output C1 , C2 & C3 will be LOW and all others will be produce the binary output "011" which represents the digital equivalent of Va. When Va is greater than 7V, C1 to C7 will be LOW and the encoder will produce "111" s the digital as equivalent of Va.

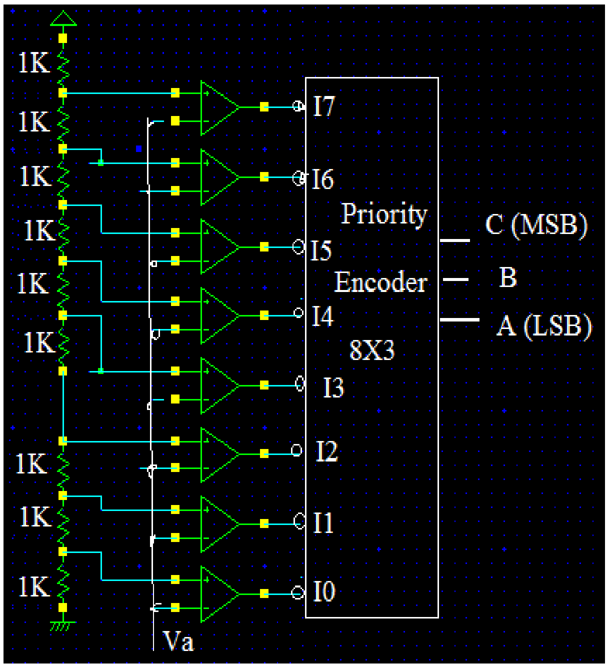

Fig 4: Flash ADC

The flash converter use no clock signal so its conversion time is very less depends only on propagation delay of the comparator and encoder.

Table 1: Fash ADC output

Analog I/P	Comparator Output	Digital Output
In Volt	Io,I1,I2,I3,I4,I5,I6, I7	CBA
0-1	1 1 1 1 1 1 1 1	000
1-2	0 1 1 1 1 1 1 1	001
2-3	0 0 1 1 1 1 1 1	010
3-4	0 0 0 1 1 1 1 1	011
4-5	0 0 0 0 1 1 1 1	100

5-6	0 0 0 0 0 1 1 1	101
6-7	0 0 0 0 0 0 1 1	110
>7	0 0 0 0 0 0 0 1	111

The most important drawback of flash ADC is that the design and hardware complexity increases exponentially by means of the resolutions since it requires a 2^N-1 comparator circuits i.e. depends on N. This as wellshows that the power dissipation and the design area increase exponentially with the resolution. The drawback is this is the analog input must drive the large nonlinear input capacitance of the comparators. Becauseof its large input capacitance, its driving current may reach up the mili Ampere range for higher frequencies which causes in large signal distortion. The third drawback is that the mismatch in the resistor reference ladder and the unequal input offset voltage of comparators limits the resolution to about 8-bit in CMOS technologies.

II. Digital Ramp ADC:

The ramp type ADC uses a counter module, voltage comparator and DAC. Here the reference voltage is connected to the comparator and when the reference voltage becomes equal to the applied input analog voltage which is to be converted, conversion will complete. For the period of this conversion process, the n bit counter store and hold the equivalent digital value to the analog input voltage (Fig 5).

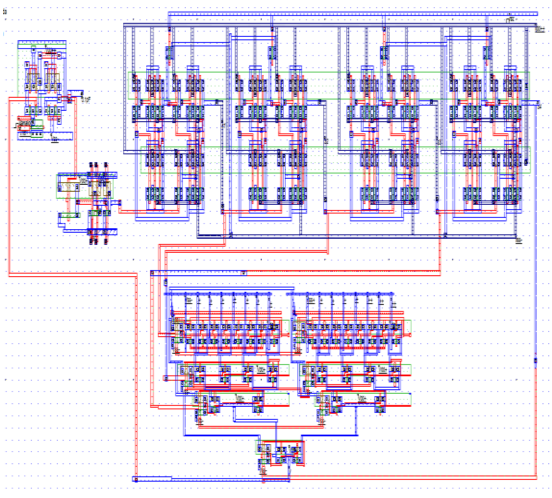

Fig 5: CMOS Layout Design for Ramp Type ADC

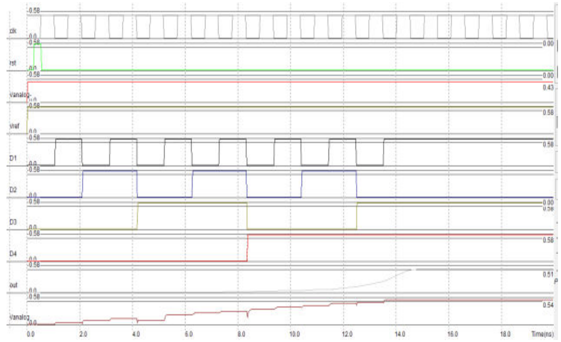

Fig 6:Timing Simulation for Ramp Type ADC

The ADC operation proceeds as follows:

1. Initially the counter is reset to "00000000" this then applied a logic HIGH signal to start the clock trigger for counter through the AND logic gate. The output of digital to analog converter is initially zero.
2. At the triggered of clock pulse through AND gate, the counter fed its output data to DAC. Thus comparator starts to compare this output of DAC with the input analog voltage applied at its noninverting terminal Va. If input Va> output of DAC Vout then the comparator output will be '1'.
3. When the output of comparator is low, this will enables the clock signal of AND gate to pass as a clock towards the counter. Thus counter start to increment its state and output at digital to analog converter increases to one step further.
4. This process is continuous until the output of of DAC becomes equal to the analog input voltage at non inverting terminal of comparator. The comparator output is now '0'. When it happens the output of comparator becomes low and this stops the clock pulse to flows a clock into the counter and counter stop to increment its states.
5. This will stop the conversion process and the data available at the output terminal of counter circuit is the equivalent converted digital data of the analog input voltage. The counter will store this equivalent digital value until another start pulse initiates a new conversion.

Dual Slop Integration ADC:

Dual slop ADC is base on integration of input analog voltage for a constant time followed by analysis of the time needed to discharge the integrating capacitor with a constant current. The time required to fully discharge the integrated capacitor is the linear function of the value of capacitor voltage at the ending of time period. This capacitor voltage is

$$V_C = \frac{1}{RiC}\int_0^T Vidt$$

$$= \frac{1}{RiC}ViT$$

During discharge time

$$V_C = \frac{1}{RiC}\int_0^T Vrefdt$$

$$= \frac{1}{RiC}Vreft$$

Thus ViT =Vref t i.e $\frac{Vi}{Vref} = \frac{t}{T}$

The time t is measured by counter, which is started immediately after time T is ended and stop by logic when the zero detector indicates that the capacitor is discharged (Fig 7).

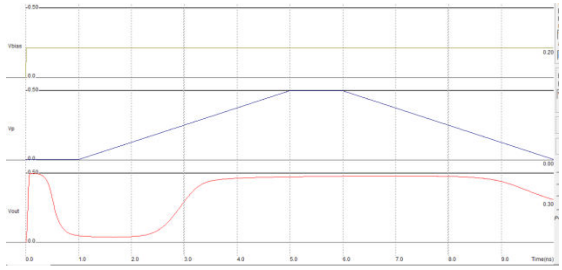

Fig 7: Timing Simulation for Dual Slop ADC

Blocks of ADC:

The blocks of ADC is design with a 8-bit voltage scaling DAC to feed digital data at comparator, a comparator logic to compare converted data with reference voltage, 8 bit digital counter to hold equivalent digital data and gate logic to pass the clock signal. In this design a pass transistor base transmission gate (TG Fig 8) is use to design the voltage scaling DAC.

The transmission gate base Voltage scaling Digital to Analog Converter (DAC) convert the analog voltage Vref to a set of 2^n voltages that are decoded to a single analog output by the input digital word.The voltage scaling is done by using series connected registers with Vref.

Transmission Gate (TG):

A transmission gate design using pass transistor MOSFETS work as an analog switch design with sourse to sourse and drain to drain connecte NMOS and PMOS transistors which are controlled by logic signals at gate terminals. When the gate terminal signal 'EN = 1' then it generates the electron channel at NMOS and holes channel at PMOS, thus conducts current from drain to source terminal and shorts the input and the output, otherwise it cuts off and the output floats.

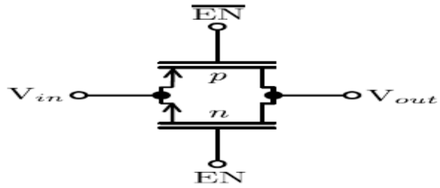

Fig 8: Transmission Gate.

The transmission gate has low ON resistance, high OFF resistance and low charge injection.Charge injection contributes three types of errors in MOS sampling circuits namely gain errors, dc offsets and nonlinearity. The reduction in charge injection is achieved due to the NMOS and PMOS devices injecting comparatively equal but opposite charge onto the load capacitor,which efficiently cancelling each other. This results in a reduction of the overall charge injection.

To enhance the speed of transmission gate its RC time constant should be small. For this the ON resistance of transmission make need to kept as small as possible. In 180nm CMOS technology the largest ON resistance of TG is observed to be 180 Ω. The on resistance of the transmission gates is inversely proportional to the W/L ratio of the transistors. For the PMOS a W/L ratio of 60:1 was used while for NMOS a ratio of 40:1 was used. The reason for the different ratios being used is because of the faster switching capabilities of the NMOS due to NMOS transistors having a higher charge carrier mobility term [5][6].

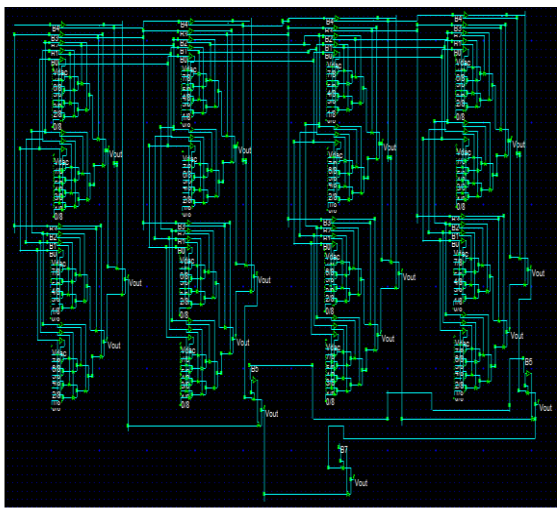

Fig 9 : Block schematic of TG base voltage scaling 8 bit DAC

The reference voltage is connected to the one input terminal of comparator circuits. When this reference voltage becomes equal to the input analog voltage at its second input, the conversion process would be complete. During this entire conversion process, the n bit counter store the digital value equivalent to the analog input voltage.

A differential circuit in design is use to restrain the noise injected by the switching regulators to the substrate and to the supply interconnects (Fig 9). These noise signals are common mode signals; they can be suppressed further by the common mode rejection of the differential circuits [3]. It converts the input voltage to a current to solve high voltage related issues and then convert back to voltage. This amplifier architecture does not use internal feedback to correct the phase margin because it is self-compensating, i.e., the larger the capacitive load on the amplifier, the greater the phase margin. Its transfer function can be expressed as

$VOUT = R1 + R2 / R1\ VB - R2 / R1\ V_{IN}$

Conclusion:

A 8 bit pipelined ADC design using Flash and Ramp ADC with transmission gate as a basic cellhas been presented in this paper. The resolution of this converter is 8 bits. The throughput of ADCs can be increased by using parallel architecture. This is verified on the circuit level with TG pass transistor circuit. The prime focus of this work is made on design and implementation of a pass transistor based TG Analog-to-Digital converter. The designed ramp type ADC is comprises of a 8-bit DAC design by transmission gate logic, a comparator logic , 8 bit digital counter and "AND" gates to pass the clock signal by considering the chip area, operation speed, and circuit complexity. In this paper, an 8-bit Sub-Ranging Analog to Digital converter (ADC) is proposed for for high-speed applications. The throughput of ADCs can be increased by using parallelism.

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