RESEARCH ARTICLE OPEN ACCESS

An Optimized CORDIC Algorithm for OFDM WPAN Application

Dr. Yogini Borole, Dr. C.G. Dethe[2]
1*(E&TC, GHRIET, SPPU Pune University, Pune*
yoginiborole@gmail.com)
2*(E&TC,UGC-Academic Staff College, Nagpur*
cgdethe@gmail.com)

Abstract:

This paper presents a technique for speed up and low-complexity using improved 2^5 512-point Fast Fourier Transform (FFT) processor utilizing an eight data path pipelined approach for high rate remote individual territory organize applications. An epic changed 2^5 FFT calculation that decreases the equipment complex nature is proposed. This strategy can diminish the quantity of complex augmentations and the size of the twiddle factor memory. It additionally utilizes a perplexing consistent multiplier rather than a complex Booth multiplier. The proposed FFT processor accomplishes a signal to-quantization commotion proportion of 32 dB at 12-bit inward word length. The proposed processor has been planned and executed utilizing 45-nm CMOS innovation with an inventory voltage of 1.2 V. The outcomes show that the absolute gate count of the proposed FFT processor is 340K. Moreover, the most noteworthy throughput rate is up to 2.8 GS/s at 420.203 MHz while requiring considerably less equipment complex nature.

Keywords — CORDIC, Modified radix2^5 FFT, OFDM, WPAN

I. INTRODUCTION

With the regularly expanding interest for mixed media applications utilizing remote transmissions over short separations, the millimetre wave (mmWave) 60 GHz remote individual zone arrange (WPAN) has been seriously investigated for a long time. Presently, the IEEE 802.11 standard Group promotion (IEEE 802.11ad) is building up a standard for the mmWave remote neighbourhood (WLAN) and WPAN systems.1 High rate WPAN frameworks will be accommodated different fast interactive media applications, for example, home system frameworks and ongoing video gushing administrations in short range indoor conditions. One key bit of leeway of IEEE 802.11ad over the other normalization exercises in the 60 GHz field is that it expands on the current solid market nearness of Wi-Fi in the 2.4/5 GHz groups. In the PHY layer structure of high rate WPANs, the symmetrical recurrence division multiplexing (OFDM) regulation has been embraced, what's more, the Fast Fourier Transform (FFT) processor is a key part. The image in the IEEE 802.11ad principles comprises of a length of 512 subcarriers. In this manner, FFT processor leads the FFT calculation with 512-point number-crunching and ought to give a highthroughput pace of at least 2.115 GS/s. As of late, there has been some exploration in the plan of multi-way pipelined FFT processors that give a high throughput [1]– [7].

Numerous FFT processor models are acquainted all together with use the OFDM transmission, for example, a single path delay commutator (SDC), multi-path delay commutator (MDC), single path delay Feedback (SDF), and multi-path delayfeedback (MDF). Among the different FFT models, the MDF engineering is every nowand again utilized as an answer for give a throughput pace of more than 1 GS/s [3]–[5]. In any case, for applications that give a throughput pace of more than 2 GS/s, the quantity of information ways can be expanded to 8 or 16, which builds the equipment cost. The zone turns out to be significantly bigger on the grounds that the memory modules are copied for the 16 information way approach. All

together to decrease the region and force utilization, a few FFT calculations also, dynamic scaling plans have been proposed [2]–[6].

The radix of the calculation significantly impacts the design of the FFT processor and the unpredictability of the implementation.Asmall radix is alluring on the grounds that it brings about a basic butterfly. By and by, a high radix diminishes the quantity of fidget factor augmentations. The radix r^kcalculations at the same time accomplish a straightforward butterfly and a decreased number of fidget factor increases [8]. The radix-2 calculation is a notable straightforward calculation for FFT processors, yet it requires numerous perplexing multipliers. The radix-4]calculation is fundamentally utilized for high information throughput FFT structures, yet requires a 4-point butterfly unit with high intricacy. As of late, the 2^4 FFT calculation furthermore, design have been concentrated so as to diminish the quantity of complex multipliers [2], [4].In this summarizing, a novel changed 2^5 FFT calculation and a 512-point FFT/IFFT processor design, which can give a high throughput of 2.8 GS/s and SQNR of 35 dB for16 QAM applications, are proposed. The key ideas for accomplishing a high information throughput, decreased equipment complication and higher SQNR execution are represented.

The association of this brief is as per the following. Part II represents the proposed changed 2^5 FFT calculation, and Part III represents the proposed 512-point 2^5 FFT design. In Section IV, the usage and examination are introduced. At long last, ends are given in Part V.

II. IMPROVED Radix 2^5 FFT PROCESS

A discrete Fourier transform (DFT) of length N is definite as follows:

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk} \ , k = 0,1, \dots, N-1 \quad (1)$$

wherever W_N is the twiddle factor and denotes the N^{th} basic origin of union, with its supporter calculated modulo N. k is the rate key and n is the period key [2]. The radix 2^5 system has the same butterfly assembly irrespective of the k importance. However, the twiddle element increase arrangement is varied with an aspect k. The 512-point FFT calculation with radix-2^k process consists of nine mathematics steps. The radix 2^k process is formulated using k-dimensional linear index mapping. The radix-2^5 algorithm can be expressed as various formulas using a common feature procedure. The radix- 2^5 procedure is given as follows.

Relating a 6-D right key chart:

$$n = \langle \frac{N}{2} n_1 + \frac{N}{4} n_2 + \frac{N}{8} n_3 + \frac{N}{16} n_4 + \frac{N}{32} n_5 + n_6 \rangle$$

$$n_1, n_2, n_3, n_4, n_5 = 0.1$$

$$n_6 = 0, \dots, \frac{N}{32} - 1$$

$$k = \langle k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5 + 32k_6 \rangle_N$$

$$k_1, k_2, k_3, k_4, k_5 = 0.1$$

$$k_6 = 0, \dots, \frac{N}{32} - 1 (2)$$

The radix 2^5 system is explaining into two breaking approaches (Scheme 1 and Scheme 2), which are called the improved radix-2^5 system. The collective reason process takings the formula of

$$\langle k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5 + 32k_6 \rangle = \sum_{n_6=0}^{\frac{N}{32}-1} \sum_{n_5=0}^{1} \sum_{n_4=0}^{1} \sum_{n_3=0}^{1} \sum_{n_2=0}^{1} \sum_{n_1=0}^{1} \times x\left(\frac{N}{2} n_1 + \frac{N}{4} n_2 + \frac{N}{8} n_3 + \frac{N}{16} n_4 + \frac{N}{32} n_5 + n_6\right) W_N^{nk}$$

$$= \sum_{n_6=0}^{\frac{N}{32}-1} \left[J_{\frac{N}{32}}(n_6, k_1, k_2, k_3, k_4, k_5) \times W_N^{(k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5)} \right] W_{\frac{N}{32}}^{n_6 k_6} \quad (3)$$

$$W_N^{\left(\frac{N}{2} n_1 + \frac{N}{4} n_2 + \frac{N}{8} n_3 + \frac{N}{16} n_4 + \frac{N}{32} n_5 + n_6\right)\left(k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5 + 32k_6\right)}$$

The scheme 1 of the improved radix 2^5 system is stated as follows:

$$= (-1)^{n1k1} (-j)^{n2k2} \quad (-1)^{n2k2} W_8^{n3(k1+2k2)}$$

$$X (-1)^{n3k3} W_{32}^{(2n4 + n5)(k1+2k2+4k3)} \quad (-1)^{n4k4} (-j)^{n5k4}$$

$$X (-1)^{n5k5} W_N^{n6 (k1+2k2+4k3+8k4+16k5)} \quad W_{N/32}^{n6k6} \quad (4)$$

The signal flow diagram for the Scheme 1 of the 64-point modified Radix-2^5 system is shown in Fig. 1(a).

The Scheme 2 of the improved radix-2^5 algorithm is stated as follows:

$$W_N^{\left(\frac{N}{2}n_1+\frac{N}{4}n_2+\frac{N}{8}n_3+\frac{N}{16}n_4+\frac{N}{32}n_5+n_6\right)(k_1+2k_2+4k_3+8k_4+16k_5+32k_6)}$$

$$X\langle k_1+2k_2+4k_3+8k_4+16k_5+32k_6\rangle = \sum_{n_6=0}^{\frac{N}{32}-1}\sum_{n_5=0}^{1}\sum_{n_4=0}^{1}\sum_{n_3=0}^{1}\sum_{n_2=0}^{1}\sum_{n_1=0}^{1} \times x\left(\frac{N}{2}n_1+\frac{N}{4}n_2+\frac{N}{8}n_3+\frac{N}{16}n_4+\frac{N}{32}n_5+n_6\right)W_N^{nk}$$

$$= \sum_{n_6=0}^{\frac{N}{32}-1}\left[J_{\frac{N}{32}}(n_6,k_1,k_2,k_3,k_4,k_5) \times W_N^{(k_1+2k_2+4k_3+8k_4+16k_5)}\right]W_{\frac{N}{32}}^{n_6 k_6} \quad (5)$$

Fig. 1(b) shows a sign stream diagram for the Scheme 2 of the 64-point changed radix-2^5 calculation. Every technique has butterfly calculation what's more, twiddle factor increase at each stage. Conditions (4) and (6) show the butterfly stages and twiddle factor increases of each stage. The twiddle factors W^n_{32} and W^n_{16} in (4) and (6) have complex numbers. On the off chance that each radix-2^5 disintegrating strategies (Scheme 1 and Technique 2) are utilized autonomously for the 512-point FFT calculation, the quantity of twiddle factor duplications will in general increment. Be that as it may, the quantity of twiddle factor duplications can be diminished by joining the Schemes 1 and 2 of the adjusted radix-2^5 calculation, which is called blended technique. Table I shows the arrangement of the 512-point FFT twiddle factor calculation at each phase for the radix-2^5FFT calculations.

For the most part, programmable complex multiplier is utilized for complex augmentations; be that as it may, if the twiddle factor has few coefficients, at that point the mind confusing constant multiplier can be utilized for the twiddle factor increases. The complicated duplication of the twiddle factors W^n_{32}, W^n_{16} and W^n_8, can be actualized in the canonic marked digit (CSD) constant multiplier, which contains the least number of non-zero digits [10]. Consequently, the area and energy utilization of the complex multipliers can be decreased. The radix-2^5 calculation has comparable complex increase design over and again every five phases. A 512-point FFT calculation utilizing radix-2^5 calculation comprises of nine phases.

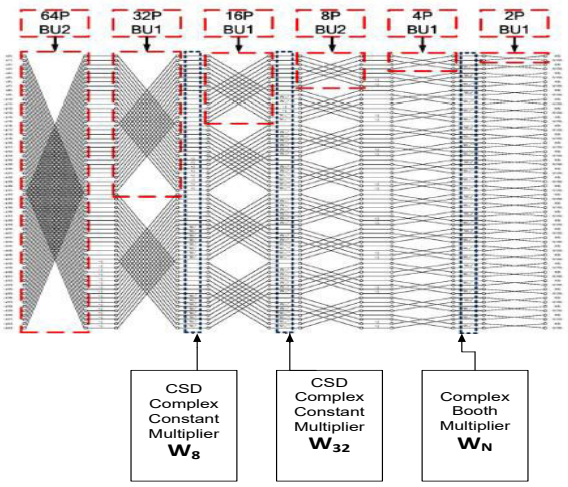

Fig. 1(a). The signal flow diagram for the Scheme 1 of the 64-point modified Radix-2^5 system

As appeared in Table I, the stage 2 in Scheme 2 has twiddle factor W_{16}, which has higher equipment unpredictability compared with W_8 in Scheme 1. Stages 7 and 8 in Scheme 1 has twiddle factors W_8 and W_{32}, which require higher equipment unpredictability analyzed to W_{16} in Method 2. In this way, the initial five phases and the other three phases use Scheme 1 and Scheme 2, individually to diminish the equipment multifaceted nature of complex multipliers, as appeared in Table I. Table II shows a correlation of the equipment unpredictability for a few eight equal data way 512-point radix-2^k MDF FFT models. Differentiated with the ordinary designs, the proposed work requires just a portion of the quantity of complex Booth multipliers. Moreover, the twiddle factor LUT requires a lot littler size thought about to the next radix-2^k calculations. To think about the equipment multidimensional nature, the complex multipliers were combined and afterward the area of separately multiplier was stabilized.

On the off chance that it is expected that the zone of the complex Booth multiplier is 1, at that point

the standardized region of the complex steady multipliers for the twiddle factor increases of W_8,W_{16}, and W_{32} is 0.12, 0.28, and 0.46, individually. The outcomes show that the proposed FFT processor utilizing the mixed system for the changed radix-2^5 calculation has the most reduced all out standardized zone of complex multiplier and littlest LUT size of fidget factor. Along these lines, it has best area throughput when differentiated with the other FFT processors.

III. PROPOSED Design

In this concise, an eight equal information way 512-point improved radix-2^5 FFT processor is proposed, as appeared in Fig. 2 (a) and Fig 2(b) represents the use of CORDIC algorithm in proposed system. There are two modules in light of the changed radix-2^5 calculation that lessen the number of twiddle factor increases. The primary module, which comprises of five handling components (PEs), is acknowledged utilizing Scheme 1 of the altered radix-2^5 calculation, and the subsequent module is acknowledged utilizing Strategy 2. The proposed design comprises of butterfly units, complex Booth multipliers, complex constant multipliers, first-in first-out (FIFO), and a control unit.

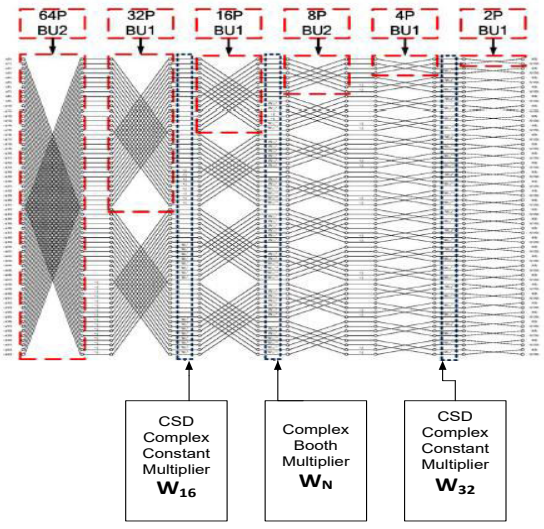

Fig. 1(b) shows a sign stream diagram for the Scheme 2 of the 64-point changed radix-2^5

A. Butterfly Units

The butterfly units perform complex increases and subtractions of two information: X[n]and X [n+ N/2]. The conduct of the butterfly units is as per the following. All info esteems are spared into the FIFO until the N/2th input is entered. At that point, the butterflyunit's direct counts between the information esteems and FIFO yields, in the wake of entering the N/2 + 1st input.During the last N/2 clock cycles, all butterfly counts are performed at each stage. Among the butterfly yields, the perplexing expansion yields are taken care of to the following stage. What's more, the complex subtraction yields are spared in the FIFO, and afterward during the following N/2 clock cycles, the FIFO yields are taken care of to the following stage. Butterfly unit 1 (BU1) conducts complex increases and subtractions as it were. Notwithstanding, butterfly unit 2 (BU2) incorporatestwiddle factor W_4 increase using the multiplexers and control signals.

The Scheme 2 of the improved radix- 2^5 process is stated asfollows:

Stage	1	2	3	4	5	6	7	8
Radix-2^2	-j	W_{512}	-j	W_{128}	-j	W_{32}	-j	W_8
Radix-2^3	-j	W_8	W_{512}	-j	W_8	W_{64}	-j	W_8
Radix-2^4	-j	W_{16}	-j	W_{512}	-j	W_{16}	-j	W_{32}
Radix-2^5	-j	W_8	W_{32}	-j	W_{512}	-j	W_8	W_{32}
	-j	W_{16}	-j	W_{512}	W_{32}	-j	W_{16}	-j
	-j	W_8	W_{32}	-j	W_{512}	-j	W_{16}	-j

TABLE I STRUCTURE OF THE 512-POINT FFT TWIDDLE FACTOR CALCULATION FOR RADIX-2^k FFT DESIGN

During the last N/2 clock cycles, all butterfly counts are performed at each stage. Among the butterfly yields, the perplexing expansion yields are taken care of to the following stage. What's more, the complex subtraction yields are spared in the FIFO, and afterward during the following N/2 clock cycles, the FIFO yields are taken care of to the following stage. Butterfly unit 1 (BU1) conducts complex increases and subtractions as it were. Notwithstanding, butterfly unit 2 (BU2) incorporatestwiddle factor W_4 increase using the multiplexers and control signals.

B. Complex Booth Multiplier with Error Compensation

The twiddle factor duplication is led utilizing fixed width complex multipliers. The twiddle factor esteems put away in the read-as it were memory (ROM) are utilized as the multiplicand in the complex Booth multiplier. The changed Booth calculation is utilized generally for fast increases. Since the most extreme clock pace of the FFT processor depends on the basic way of the complex Booth multiplier, three-level pipelined complex Booth multiplier is utilized for fast activity. Since quantization mistakes influence the signal to noise ratio (SNR) execution of the framework, a mistake pay technique [9] is utilized to diminish the quantization mistake.

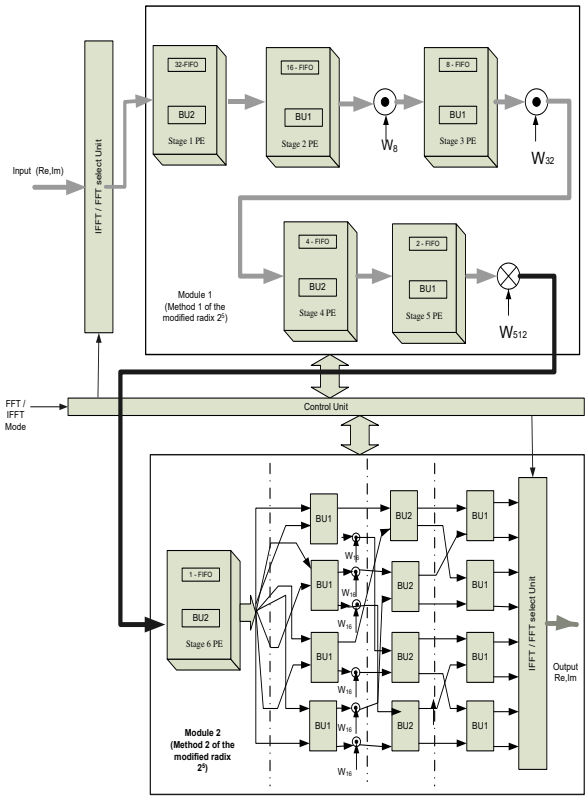

Fig.2(a) Proposed improved radix-2^5 512-point FFT processor

C. Complex Constant Multiplier

The proposed FFT processor utilizes steady multipliers dependent on the canonical signed digit (CSD) representation for the complicated arithmetic calculations in stages 2, 3, and 7. The twiddle factor W_8 has as it were one coefficient, yet fidget factors W_{16} and W_{32} have three and seven coefficients, separately. For the most part the current research is utilizing complex Corner multipliers for the twiddle factor W_{32} increase. In any case, in our structure, the complex CSD constant multiplier has been utilized for the twiddle factor W_{32} increase. Likewise, the basic sub-articulations sharing (CSS) strategy lessens the equipment multifaceted nature of the complex CSD steady multipliers [10], as appeared in Fig. 4. The steady multiplier utilizing the CSS procedure is executed utilizing the basic estimation designs X1, X2, and X3. The proposed FFT processor applied CSD steady multiplier rather than complex Booth multiplier at a few phases. Therefore, the equipment intricacy of complex multiplier is diminished by in any event 80% in correlation with utilizing complex Booth multiplier. Also, the twiddle factor LUT size is diminished to 90% differentiated with the structures utilizing the intricate Booth multipliers.

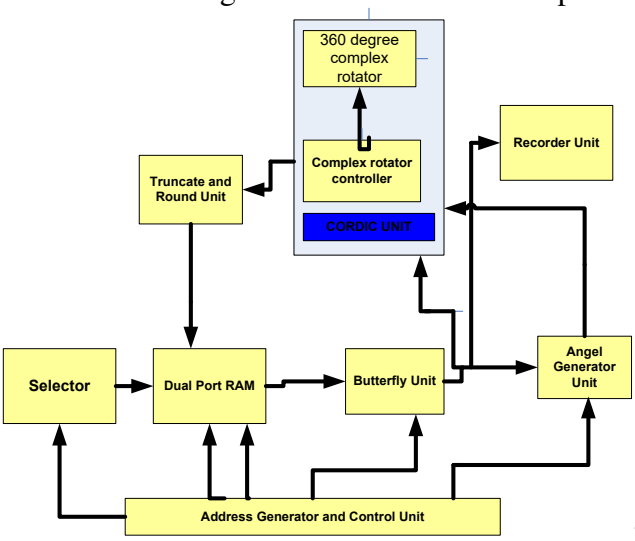

Fig 2(b) Use of CORDIC algorithm in proposed system

RESULT

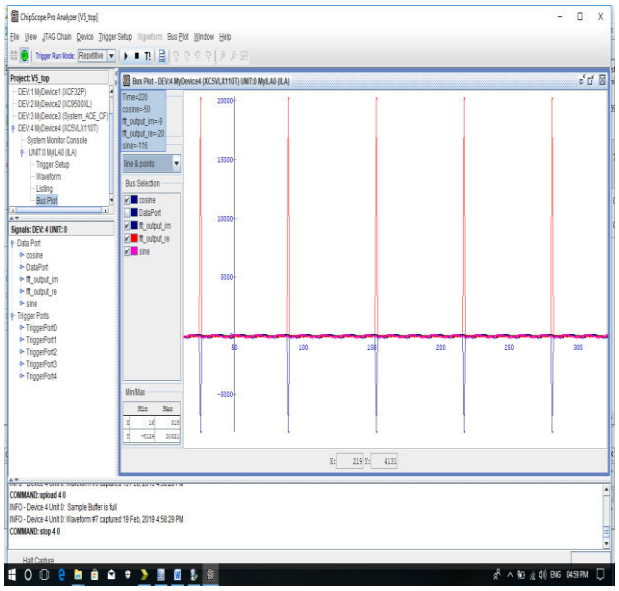

Fig.3(a) Bus Plot output

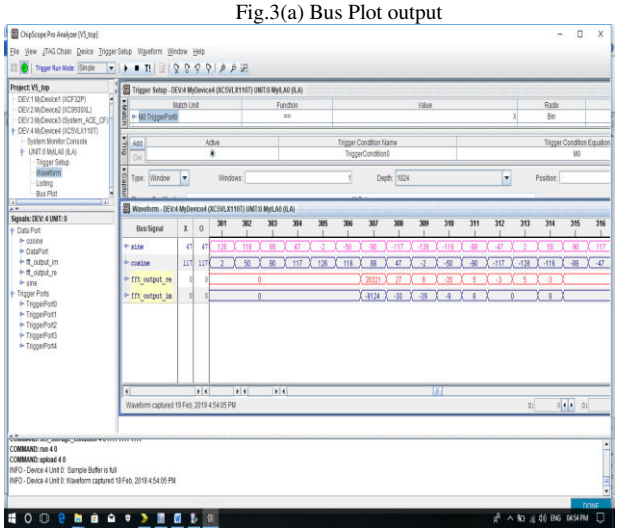

Fig.3(b) Chip Scope Pro Analyser output

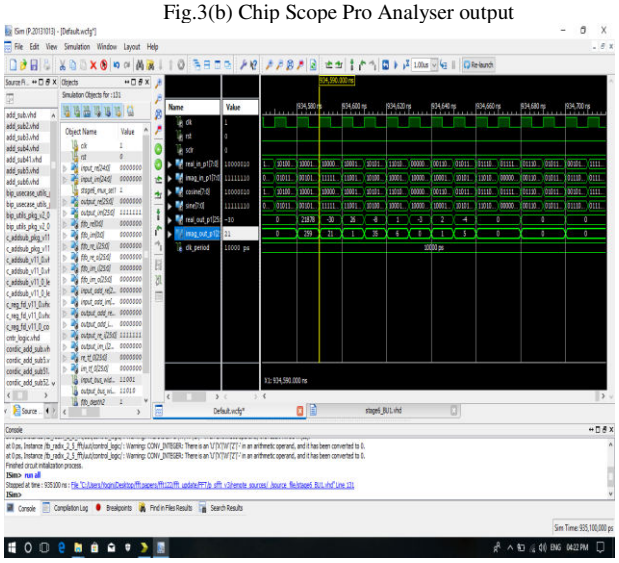

Fig.3(c) Simulation Result

Table II a correlation of the equipment unpredictability for a few eight equal data way 512-point radix-2^k MDF FFT models.

Parameters	Proposed	[3]	[5]	[6]
FFT size	512	2048	2048	512
Technology	90nm	90nm	90nm	90nm
FFT algorithm	Modified radix 2^5 with CORDIC	Mixed radix	Mixed radix	Radix - 16
No of Data Paths	8	4	8	16
Architecture	MDF	MDF	MDF	Memory based
Gate Count	340K	-	-	-
Memory	504	2044	2040	512
Max.Clock Frequency	420.203	300	300	324
Through put	2.8	1.2	2.4	2.6
Power Consumption mW	98.8	117	159	103.5

CONCLUSION

In this paper, the effective equipment engineering of FFT calculation for Advanced OFDM applications is proposed.In thispaper,thepossibilitiestoimprovethecomplexity andtheperformanceoftherotationsinFFTsatalgorithmicandarithmeticlevelwereinvestigated.Aframeworkforthegenerationofalargenumberofpossible FFTalgorithmshasbeenproposed.Basedonthisframework,thegeneratedFFTalgorithmswillhavethesamebutterflyoperationsanddataflow,butdifferinthetwiddlefactormultiplication.Thedifferenceamongthese FFTalgorithmsliesintermsofswitchingactivityofthetwiddlefactormultiplication,thenumberofnon-trivialmultiplications,thecoefficientmemorycomplexity,andtheround-offnoise,whicharerelatedtothepowerconsumption,areaandperformanceofthecircuit.The proposed architecture includes modified radix 2^5 FFT with CORDIC algorithm together, which can at a time provide reduction in latency and the increment of throughput. The number of complex booth multipliers and twiddle factor LUTs are reduced using modified radix 2^5 FFT with CORDIC algorithm. Modified radix 2^5 FFT processor the most area-efficient architecture for the eight parallel 512-point MDF FFT processors. The highest throughput rate is up to 2.8 GS/s at the clock frequency of 420.203 MHz. The entire 512-bit architecture operates at a clock frequency of

420.203 MHz with total gate count of 340k. The results compared with Xilinx FPGA Virtex-5 and chip Scope pro software.

REFERENCES

[1] Taesang Cho and Hannho lee, "A High-Speed LowComplexity Modified Radix-2^5 FFT Processor for High Rate WPAN Application" IEEE Trans. VLSI SYSTEMS, vol.21, no. 1, JANUARY 2013.

[2] J. Lee and H. Lee, "A rapid two-equal FFT/IFFT processor for MB-OFDMUWB Systems," IEICE Trans. Fundam., vol. E91-A, no. 4, pp. 1206–1211, Apr. 2008.

[3] Y. Lin, H. Liu, and C. Lee, "A 1-GS/s FFT/IFFT processor for UWB applications," IEEE J. Strong State Circuits, vol. 40, no. 8, pp.1726–1735, Aug. 2005.

[4] Y. Chen, Y. Tsao, Y. Wei, C. Lin, and C. Lee, "An ordered scaling pipelined FFT processorfor OFDM-based WPAN applications," IEEE Trans. Circuits Syst.II, Exp. Briefs, vol. 55, no. 2, pp. 146–150, Feb. 2008.

[5] M. Shin and H. Lee, "A fast four-equal FFT processor for UWB applications," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 2008, pp. 960–963.

[6] S.Tang, J. Tsai, and T. Chang, "A 2.4-GS/s FFT processorfor OFDM based WPAN applications," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 6, pp. 451–455, Jun. 2010.

[7] Huang and S. Chen, "A green FFT processor with 2.5-GS/s for IEEE 802.15.3c (WPANs)," in Proc. Int. Conf. Green Circuits Syst. (ICGCS), 2010, pp. 9–13.

[8] T. Cho, H. Lee, J. Park, and C. Park, "A fast low-intricacychanged radix-25 FFT processor for gigabit WPAN applications," in Proc. IEEE Int. Symp. Circuits Syst.(ISCAS), 2011, pp. 1259–1262.

[9] A. Cortes, I. Velez, and J. F. Sevillano, "Radix FFTs:Matrical portrayal and SDC/SDF pipeline usage," IEEE Trans. Signal Process., vol. 57, no. 7, pp. 2824–2839, Jul. 2009.

[10] K.Cho, K. Lee, J. Chung, and K. Parhi, "Structure of low-mistake fixed width changed Booth multiplier," IEEE Trans.Very Large Scale Integer. (VLSI) Syst., vol. 12, no. 5, pp. 522–531, May 2004.

[11] R. I. Hartley, "Sub articulation partaking in channels utilizing canonic marked digit multipliers," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 43, no. 10, pp. 677–688, Oct. 1996.

[12] Wey, C., Lin, S., and Tang, W. (2007). Productive memory-based FFT processors for OFDM applications. In IEEE International Conf. on Electro-Information Technology, 345–350.May

[13] Fanucci, L., Forliti, M., and Gronchi, F. (1999). Single-chip blended radix FFT processor for continuous on-board SAR handling. In sixth IEEE International Conference on Electronics, Circuits and Systems, 2, 1135–1138.

[14] Mittal, S., Khan, M., and Srinivas, M. B. (2007). On the appropriateness of Bruun's FFT calculation for programming characterized radio. In 2007 IEEE Sarnoff Symposium, (pp. 1–5), Apr.

[15] Volder, J. (1959). The CORDIC trigonometric processing procedure. IEEE Transactions on Electronic Computers, 8(8), 330–334.

[16] Despain, A. M. (1974). Fourier change PCs utilizingCORDIC emphasess. IEEE Transactions on Electronic Computers, 23(10), 993–1001.

[17] Abdullah, S. S., Nam, H., Mc Dermot, M., and Abraham, J. A. (2009). A high throughput FFT processor without any multipliers. In IEEE International Conf. on Computer Design, pp. 485–490.

[18] Lin, C., and Wu, A. (2005). Blended scaling-turn CORDIC (MSRCORDIC) calculation and engineering for elite vector rotational DSP applications. Frameworks I, 52(11), 2385–2396.

[19] Jiang, R. M. (2007). A zone productive FFT design for OFDM advanced video broadcasting. IEEE Transactions on Consumer Electronics, 53(4), 1322–1326.

[20] Garrido, M., and Grajal, J. (2007). Effective memory-less CORDIC for FFT Computation. In IEEE International Conference on Acoustics, Speech and Signal Processing, 2, 113-116), Apr.

[21] Xiao, X., Oruklu, E., and Saniie, J. (2009). Quick memory tending to conspire for radix-4 FFT usage. In IEEE International Conference on Electro/Information Technology, EIT 2009, 437–440, June.

[22] Xiao, X., Oruklu, E., and Saniie, J. (2010) Reduced Memory Architecture for CORDIC-based FFT. In IEEE International Symposium on Circuits and Systems, 2690–2693.

[23] MaY.(1999). A viable memory tending to conspire for FFT processors. IEEE Transactions on Signal Processing, 47(3), 907–911.