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Power Reduction of Domino Logic with clock gating using 16nm CMOS Technology

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Abstract:

In this paper, a new technique of power reduction in CMOS domino logic is proposed. The proposed technique uses clock gating as well as output hold circuitry. Clock is passed to the domino logic only during the active state of the circuit. During standby mode, clock is bypassed while the state of the circuit is retained. A 2:1 multiplexer is used for clock gating and for retaining the state of the circuit. Simulation results are being carried out in a 2-input NAND gate, 2-input nor gate and 1-bit conventional full adder cell in 16nm CMOS technology. The power of the proposed circuit is reduced to an average of 99.37 % with respect to standard domino logic. Propagation delay is slightly increased to an average of 4.53 %. Area of the proposed circuit increases to four transistors per domino module.

Keywords — Dynamic, Domino, static power, clock gating, CMOS.

I. INTRODUCTION

The modern technologies move towards smaller, faster, and cheaper computing systems. This has been facilitated by exponential increase in device density and operating frequency through VLSI technology scaling. This has led to an increase in power consumption that has reached limits of reliability and cost. In addition, continued scaling into the nanometer system has brought design robustness issues such as soft error, signal integrity, and process variability. In addition, the issues of power consumption and robustness are affected with time. This has created a predicament in computer system design that intimidated to be an uncertain block to future advancement [2].

The fast improvement of VLSI CMOS circuit technique is due to the wireless systems with low power budgets and increased use of small sized gadgets and very high speed processors. To attain this requirement, the supply voltages and size of transistors are scaled with technology. Due to larger number of devices per chip, the interconnection density increases [3]. The interconnection density along with high clock frequency increases capacitive coupling of the circuit. Therefore, the noise pulses are generated leading to logic failure and delay of the circuit [6]. Again, when supply voltage is scaled, the threshold voltage of the device needs to be scaled to preserve the circuit performance, which leads to increase in the leakage current of the device Due to low device count and high speed especially compared to complementary CMOS, dynamic-logic circuits are broadly used in a wide range of applications including dynamic memory, digital signal processors and microprocessors. Dynamic circuit contains a pull-down network which realizes our desired logic functions. According to the basic dynamic circuit operation, the dynamic node precharges at every clock cycle. As the clock signal frequency is high, the circuit generates a lot of noise which consumes extra power and slows the circuit.

II. LITERATURE SURVEY

A domino logic module consist of a pull down network (PDN), dynamically connected, followed by a static inverter [7] as shown in figure 1. The non-inverting output of domino is represented by

signal out while domino node is represented by X. The PDN is built exactly as that in complementary CMOS.

A. Standard Domino Logic Module

The domino module works in two phases - precharge and evaluation, where the signal clock controls the mode of operation as shown below:

$$clock = \begin{cases} 0, & \text{precharge phase} \\ 1, & \text{evaluation phase} \end{cases}$$

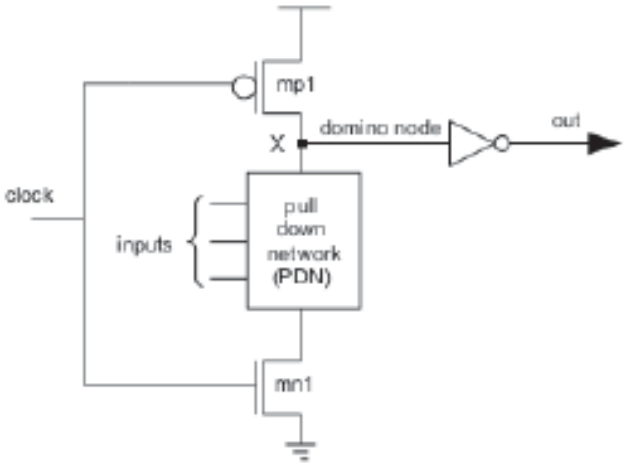

Figure: A Standard Domino Logic Module

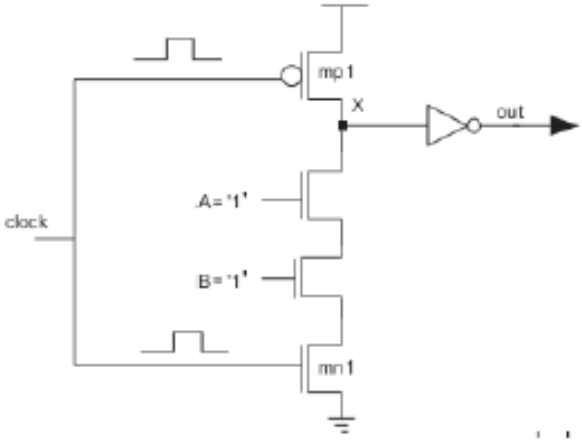

Figure: NAND gate using domino logic

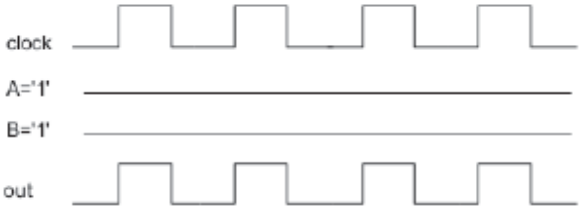

Figure: Waveforms for a 2-input NAND gate using domino logic during standby mode

During precharge phase, domino node X is charged to VDD by pmos transistor mp1. The nmos transistor mn1 is off during this phase. During evaluation phase, transistor mp1 is off while mn1 is in on state. If the input values are such that PDN conducts, node X discharges, otherwise it will hold the precharge value i.e. VDD. Figure 2 shows the domino logic module for a 2-input nand gate. Let the inputs of a 2-input nand gate domino logic are '11' i.e. A='1' and B='1' during standby mode. For this case, the out should be '1' but since the clock is present, out is a pulse as shown in figure 3. The presence of clock and the pulse shaped output dissipates a significant amout of power dissipation during standby mode. For the other combinations of standby inputs i.e. '00, '01' and '10', out is '0'. The presence of clock in domino logic leads to power dissipation in this case. Domino logic is faster than its static logic counterparts. Although, it is very sensitive to noise sources such as leakage current, crosstalk, charge sharing, power supply bump and ground bounce since its dynamic node cannot be recovered after the data is lost by those noise sources [4,5].

III. PROPOSED SYSTEM

We have presented a new scheme for the design of noise tolerant domino logic technique. This circuit contains a precharge transistor, an evaluation network, footer transistors and semi-dynamic inverter as depicted in figure. In the precharge period when the clock is low, the precharge pmos gets on and dynamic node is connected to v_{dd} and gets precharge to v_{dd}. When clock goes high, the evaluation phase starts and output gets evaluated with pull-down network that conditionally gets discharged if the pdn is on. During evaluation period when all the inputs are at logic 0, the

dynamic node stays at logic 1. However, in case of wide fan-in circuits, due to the sub threshold leakage pdn network leaks the charge stored in the capacitance at the dynamic node. When a noise voltage impulse occurs at gate input, voltage level of the dynamic node decreases resulting is change in output logic [8,9]. To stop that, the footer transistors (m_2, m_3 and m_4) are connected. M_3 acts as stacking transistor [10,11]. At the evaluation period, when the dynamic node should be discharged, at that time m_2 makes a charge discharge path. In basic domino logic, the output pulses persist in the circuit, due to the precharge act.

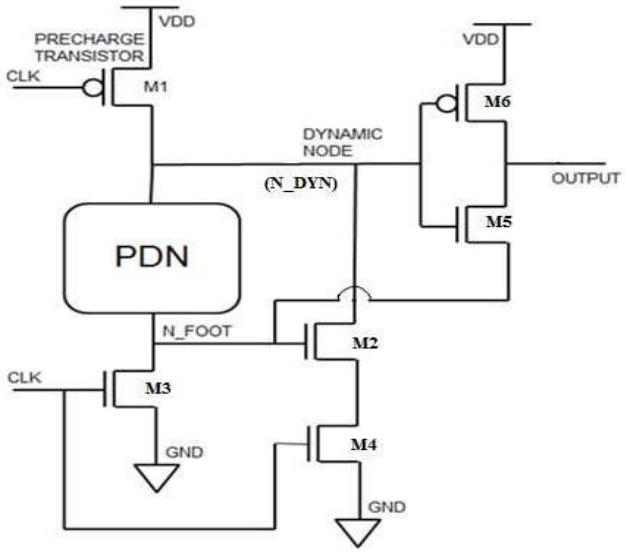

Figure: Proposed Circuit

The pulses of output node N_FOOT always propagated because of turning on the NMOS transistor present in the buffer by precharge pulse in the dynamic node. Therefore it can be easily said that we can avoid the precharge pulse propagating to the output of the buffer, if we can turn off the NMOS transistor of the buffer during precharge. Following this method, this unique circuit technique is proposed [13].

B. Circuit Analysis

The proposed novel domino circuit scheme is shown in Figure. Transistor M_3 is used as stacking transistor. Due to voltage drop across M_3, gate-to-source voltage of the NMOS transistor in the PDN decreases. The proposed circuit has additional evaluation transistor M_4 with gate connected to the CLK. When M_3 has voltage drop due to presence of noise-signals, M_2 starts leaking which causes a lot of power dissipation. This makes the circuit less noise robust. In proposed scheme, the transistor M_4 causes the stacking effect, which makes gate-to-source voltage V_{GS} of M_2 smaller (M_3 less conducting). Hence circuit becomes more noise robust and less leakage power consuming.

C. Noise Analysis

When PDN is OFF and the N_DYN is at high voltage, at that time the N_FOOT stays at low voltage. Due to the high voltage level of dynamic node, the gate of the NMOS (M_5) goes high and the low level of N_FOOT makes the source of the M_5 to 0. This makes M_5 ON and voltage of buffer output becomes same as the voltage of N_FOOT. It can be easily verified that if the NMOS transistor of buffer can be turned off permanently, by doing this, the pulses propagating to the output can be avoided. In the evaluation period, when the NMOS M_3 is ON, N_FOOT gets discharged to 0. When PDN is ON the N_DYN also gets discharged to ground. This makes the V_{GS} of buffer NMOS M_5 to 0 as $V_{GS}=V_G-V_S=0$. This results in switching OFF the NMOS and the buffer output gets completely charged through PMOS M_6.

In precharge the dynamic node will get charged to high, when PDN is ON the voltage of the N_FOOT is nearly same as N_DYN, as the NMOS M_3 is OFF. The V_{GS} of the buffer NMOS will be $V_G - V_S < V_{TH}$ which keeps the NMOS of the buffer at turned OFF stage. The PMOS of the buffer is also OFF due to the high level of N_DYN node. This makes the output of buffer LOW [14].

D. Power Analysis

The proposed structure uses semi-domino buffer structure. So the output node OUT has no pulses in precharge stage as shown in Figure. In the figure the first waveform shows the clock the second and third wave form shows the waveform of the input signals namely A and B.

IV. RESULTS

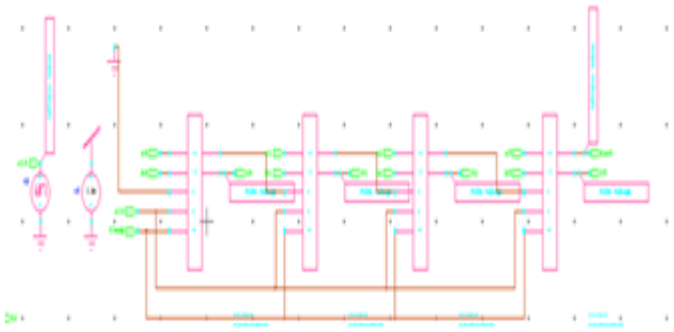

Figure: Proposed Circuit for 16nm 4bit Domino ADDER

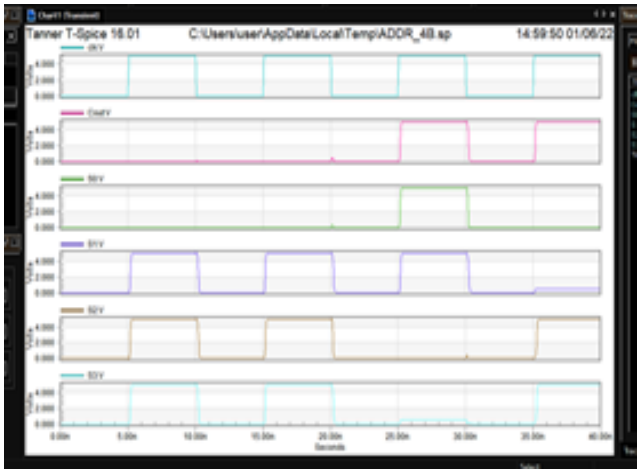

Figure: 2. Proposed Circuit 16nm Waveforms

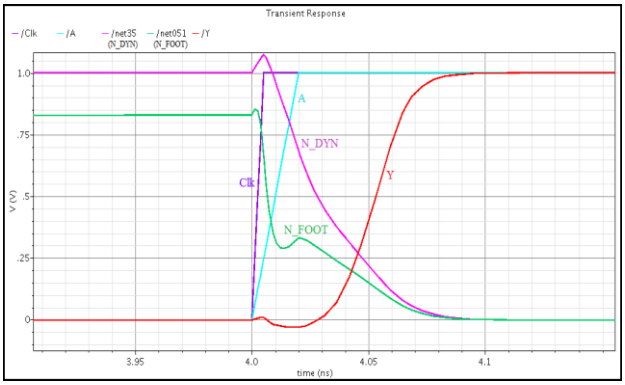

Figure: Simulated waveform of proposed scheme

V. CONCLUSION

In this dissertation, we have introduced and demonstrated a novel logic style. This logic consumes low power and is noise robust. This proposed logic is superior to domino and static CMOS logic in addition to some recent proposed logic styles in terms of energy and delay, and at the same time is more noise robust than any logic styles. In particular, we have shown 60 – 80 % power reduction vs. domino and 30 – 50 % speed improvement vs. static CMOS. In addition, we have presented that the logic also works efficiently with sequential circuits.

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